DEPARTMENT OF THE ARMY TECHNICAL MANUAL **TM 11-5805-424-15**

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DEPARTMENT OF THE AIR FORCE TECHNICAL ORDER **TO 31W2-2G-41**

OPERATOR'S

ORGANIZATIONAL, DS, GS

AND DEPOT MAINTENANCE MANUAL

MODEM LOW SPEED

WIRE LINE MD-674(P)/G

(NSN 5805-00-963-4888)

This copy is a reprint which includes current pages from Changes 1 through 5.

DEPARTMENTS OF THE ARMY, THE NAVY, AND THE AIR FORCE

JUNE 1967

WARNING

HIGH VOLTAGE

is used
in this equipment.

DEATH ON CONTACT

may result if safety precautions
are not observed.

Be careful not to contact high voltage connections or any power connections when using this equipment. Turn off the power and discharge all high voltage capacitors before making any connections or doing any work inside the equipment. Be extremely careful when working on, or near transformer T1 of the power supply.

EXTREMELY DANGEROUS VOLTAGES UP TO 230 VOLTS EXIST IN THE POWER SUPPLY SECTION OF THE EQUIPMENT

DO NOT TAKE CHANCES!

TECHNICAL MANUAL
NO. 11-5805-424-15
TECHNICAL PUBLICATION
NAVELEX 0967-220-9010
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DEPARTMENTS OF THE ARMY,

THE NAVY, AND THE AIR FORCE

WASHINGTON, DC, *19 June 1967*

OPERATOR'S, ORGANIZATIONAL, DIRECT SUPPORT, GENERAL SUPPORT, AND DEPOT MAINTENANCE MANUAL

MODEM, LOW SPEED WIRE LINE, MD-674(P)/G (NSN 5805-00-963-4888)

REPORTING ERRORS AND RECOMMENDING IMPROVEMENTS

You can help improve this manual. If you find any mistakes or if you know of a way to improve the procedures, please let us know. Mail your letter or DA Form 2028 (Recommended Changes to Publications and Blank Forms) direct to: Commander, US Army Communications-Electronics Command and Fort Monmouth, ATTN: AMSEL,-ME-MP, Fort Monmouth, New Jersey 07703-5007.

For Air Force, submit AFTO Form 22 (Technical Order System Publication Improvement Report and Reply) in accordance with paragraph 615, Section VI, T.O. 00-5-1 Forward direct to prime ALC/MST.

For Navy, mail commends to the Commander, Naval Electronics Systems Command, ATTN: ELEX 8211, Washington, DC 20360.

In either case, a reply will be furnished direct to you.

LIST OF ILLUSTRATIONS

FOLD-IN ILLUSTRATIONS

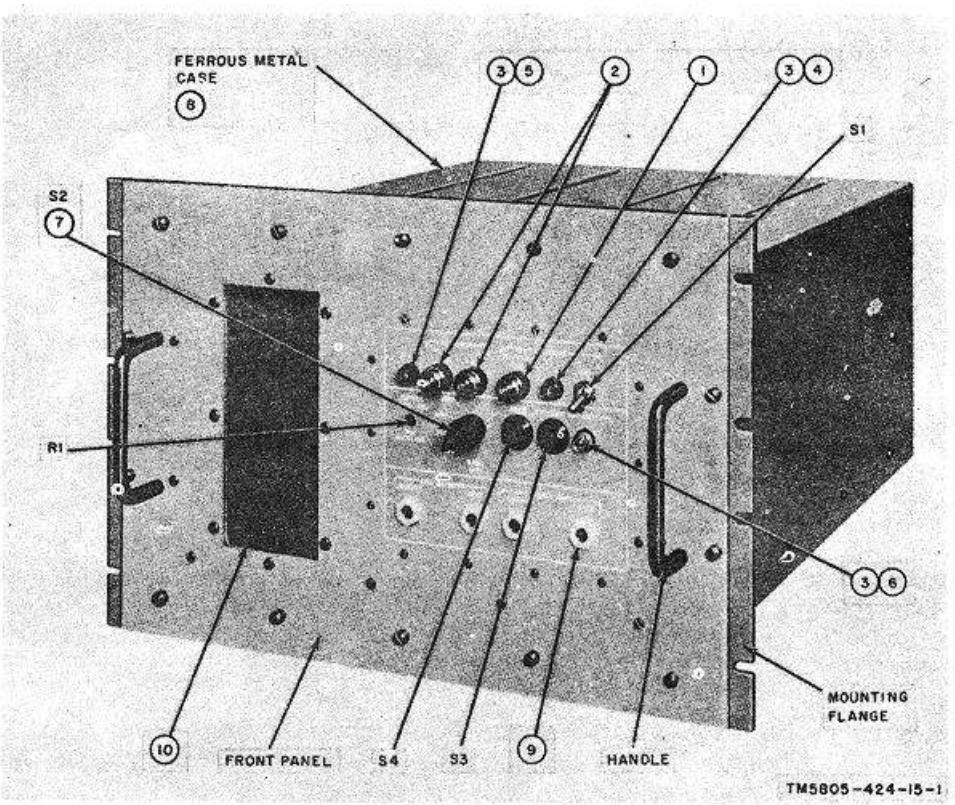


Figure 1-1. Modem, Low Speed Wire Line MD-474(P)/G.

CHAPTER 1

INTRODUCTION

Section I. GENERAL

1-1. Scope

a. This manual describes Modem, Low Speed Wire Line MD-674(P)/G (fig. 1-1), and covers its installation, operation, and maintenance. It includes instructions for operation under usual and unusual conditions, and also includes detailed functioning of the equipment.

b. Official nomenclature followed by (*) is used to indicate all subassemblies of the equipment covered in this manual. Thus, Modem Subassembly MX-73(*)/G represents Modem Subassemblies MX-7372/G, MX-7373/G, MX-7374/G, MX7375/G, MX-7376/G, MX-7377/G, MX-7378/G, MX-7379/G, MX-7380/G, MX-7381/G, MX7382/G, MX-7383/G, MX-7384/G, MX-7385/G, and MX-7386/G.

1-2. Consolidated Index of Army Publications and Blank Forms

Refer to the latest issue of DA Pam 310-1 to determine whether there are new editions, changes or additional publications pertaining to the equipment.

1-3. Maintenance Forms, Records, and Reports

a. Reports of Maintenance and Unsatisfactory Equipment. Department of the Army forms and procedures used for equipment maintenance will be those prescribed by DA Pam 738-750, as contained in Maintenance Management Update. Air Force personnel will use AFR 66-1 for maintenance reporting and TO-00-35D54 for unsatisfactory equipment reporting. Navy personnel will report maintenance performed utilizing the Maintenance Data Collection Subsystem (MDCS) IAW OPNAVINST 4790.2, Vol 3 and unsatisfactory material/conditions (UR submissions) IAW OPNAVINST 4790.2, Vol 2, chapter 17.

b. Report of Packaging and Handling Deficiencies. Fill out and forward SF 364 (Report of Discrepancy (ROD)) as prescribed in AR 735-11-2/DLAR 4140.55/ NAVMATINST 4355. 73A/AFR 400-54/MCO 4430.3F.

c. Discrepancy in Shipment Report (DISREP) (SF 361). Fill out and forward Discrepancy in Shipment Report (DISREP) (SF 361) as prescribed in AR 55-38/ NAVSUPINST 4610.33C/AFR 75-18/ MCO P4610.19D/ DLAR 4500.15.

1-3.1 Deleted

1-3.2. Administrative Storage

Administrative storage of equipment issued to and used by Army activities will have preventive maintenance performed in accordance with the PMCS charts before storing. When removing the equipment from administrative storage the PMCS should be performed to assure operational readiness. Disassembly and repacking of equipment for shipment or limited storage are covered in chapter 2 and TM 740-90-1.

1-3.3. Destruction of Army Electronics Materiel

Destruction of Army electronics materiel to prevent

enemy use shall be in accordance with TM 750-244-2.

1-3.4. Reporting Equipment Improvement Recommendations (EIR)

a. Army. If your equipment needs improvement, let us know. Send us an EIR. You, the user, are the only one who can tell us what you don't like about your equipment. Let us know why you don't like the design. Put it on an SF 368 (Quality Deficiency Report). Mail it to Commander, US Army Communications-Electronics Command and Fort Monmouth, ATTN: AMSEL-ME-MP, Fort Monmouth, New Jersey 07703-5007. We'll send you a reply.

b. Air Force: Air Force personnel are encouraged to submit EIR's in accordance with AFR 900-4.

c. Navy. Navy personnel are encouraged to submit EIR's through their local Beneficial Suggestion Program.

Section II. DESCRIPTION AND DATA

1-4. Purpose and Use

a. The MD-674(P)/G provides a single-channel terminal facility for transmission of serial digital information over a four-wire, voice-frequency (vf) circuit (fig. 1-9). The MD-674(P)/G may use Clock Module Group OA-8072/G to supply a stable station clock signal, as shown at site A; or a station clock signal from another equipment, as shown at site B. MD-674(P)/G's may be used to provide multiplex terminal facilities (fig. 1-10) if each MD-674(P)/G utilizes a different Modem Subassembly MX-73(*)/G (*b* below), and the combined baud rate of the MD-674(P)/G's does not exceed 1,200 baud (*c* below). Two MD-674(P)/G's may also be used as a repeater facility in a single channel system (no multiplexing) as shown in figure 1-11. Multiple channel repeater facilities may be used in multiplex systems by use of two MD674(P)/G's (back-to-back) for each channel. An order-wire teletypewriter communications facility is provided with an automatic break-in.

b. The baud rate and audiofrequency of the MD-674(P)/G are determined by the type of Modem Subassembly MX-73(*)/G installed in the MD-674(P)/G. The chart below indicates the MX-73(*)/G's available for each baud rate, the voice frequency of each MX-73(*)/G, and indicates whether delay equalization is fixed, optional, or adjustable with the MX-73(*)/G. Any MX-73(*)/G may be used for any baud rate below its baud rate. That is, a 600 baud MX-73(*)/G may be used for a 300 or 150 baud rate with the channel frequencies remaining the same for each rate.

		Audiofrequency (cps)			
Baud rate	*MX-73(*)/G*	*Mark*	*Center*	*Space*	*Delay equalization*
150	MX-7372/G	425	10	595	Fixed.
	MX-7374/G	765	850	935	Fixed.
	MX-7376/G	1,105	1190	1,275	Fixed.
	MX-7378/G	1,445	1,553	1,615	Fixed.
	MX-7380/G	1,785	1,870	1,955	Fixed.
	MX-7382/G	2,125	2,210	2,295	Fixed.
	MX-7384/G	2,465	2,550	2,635	Fixed.
	MX-7386/G	2,805	2,890	2,975	Fixed.
300	MX-7373/G	510	80	850	Optional.
	MX-7377/G	1,190	1,360	1,530	Fixed.
	MX-7381/G	1,870	2,040	2,210	Fixed.
	MX-7385/G	2,550	2,720	2,890	Optional.
600	MX-7375/G	680	1,020	1,360	Optional.
	MX-7383/G	2,040	2,380	2,720	Optional.
1,200	MX-7379/G	1,200	1,800	2,400	Adjustable.

Type:
Synchronous ..... Up to 1,200 baud.
Asynchronous..... Up to 1,200 baud limited by MX-73(*)/G installed in unit.
Voltage levels,
Input'
Data 1
(mark) ..... +0.5 to +7.0 volts.
Data 0
(space)..... -0.5 to -7.0 volts.
Output:
Date 1
(mark) ..... +6 Volts ±1.
Data 0
(space)..... -6 volts ±1.
Alarms ..... Activates with lack of digital data for 5 seconds (input or output).
Data frequencies:
150 baud ..... 510 cps ±85,850 cps ± 85, 1,190 cps ±85, 1,530 cps ±85, 1,870 cps ±85, 2,210 cps ± 85, 2,550 cps ±85, or 2,890 cps ±85.
300 baud ..... 680 ±170, 1,360
(or 1501..... cps ±170, 2,040 cps ± 170, or 2,720 cps ±170.
600 baud ..... 1,020 ±340 or
(or 300 or 150) 2,380 cps ±340.
1,200 baud..... 1,800 cps ±600.
(or 600, 300 or 150)
Impedance:
Input ..... 6,800 ohms ±68.
Output ..... Less than 100 ohms.

b. Vf Input and Output Signals.

Impedance..... 600 ohms ±6, balanced and grounded.
Level:
Output..... -20 to +3 dbm (continuously adjustable).
Input..... -35 to +7 dbm.
Frequency stability..... Within one part in 105 per day.
Order wire:
Output..... Carrier signal interruption for 1.5 seconds ±0.25.
Input..... Response to carrier interruption between 1.25 and 1.75 seconds.
Alarms:
Output..... Activates when level drops 10 db or more from preset level for 2 seconds (adjustable); resets when level returns to within 5 db of preset level.
Input Activates ..... Activates when level drops 20 db or more from preset level for 2 seconds (adjustable) reacts when level returns to within 10 db of preset level.

c. Clock Timing Signal.

Stability ..... Less than 1/2-bit drift for transmission interruption up to 30 minutes
Impedance..... Less than 100 ohms
Transmit timing..... Two uncorrected outputs balanced within 10 percent of each other within +6 to -6 volts.
Receive timing..... Two phase-corrected outputs within 2 percent of center of data bit negative zero crossing.

All data on pages 1-4 through 1-4.3 are deleted.

1-7. Description

The MD-674(P)/G (fig. 1-2) consists of one MX-73(*)/G as determined by the site of requirements, and may contain the OA-8072/G, if the MD-674(P)/G is used to supply the station clock signal (para 1-4). The MD-674(P)/G is also supplied with running spares (fig. 1-3) to insure minimum downtime. The MD-674(P)/G may be mounted in a standard, 19-inch rack and contains a drawer-type chassis (fig. 1-4). A printed-circuit (PC) card nest (fig. 1-6) contains all operating printed circuit cards. Special compartments are provided for the MX-73(*)/G and the OA-8072/G (fig. 1-6). The bottom view of the MD-674(P)/G is shown in figure 1-7 and the rear view is shown in figure 1-8.

1-8. Circuit Boards for Different MX-73(*)G Units

The following list identifies printed circuit boards (PCB's) used for the different MX-73(*)/G Modem Subassemblies.

MX-73(*)G	*PCB*	*NSN*
MX-7372/G, MX-7373/G	D80034200	5805-00-916-9630
MX-7374/G, MX-7375/G, MX-7376/G	D80034190	5805-00-916-9631
MX-7377/G, MX-7378/G, MX-7380/G	D80034180	5805-00-916-9632
MX-7381/G, MX-7382/G, MX-7383/G	D80034180	5805-00-916-9632
MX-7379/G	D80034230	5805-00-916-9629
MX-7384/G, MX-7385/G, MX-7386/G	None.	

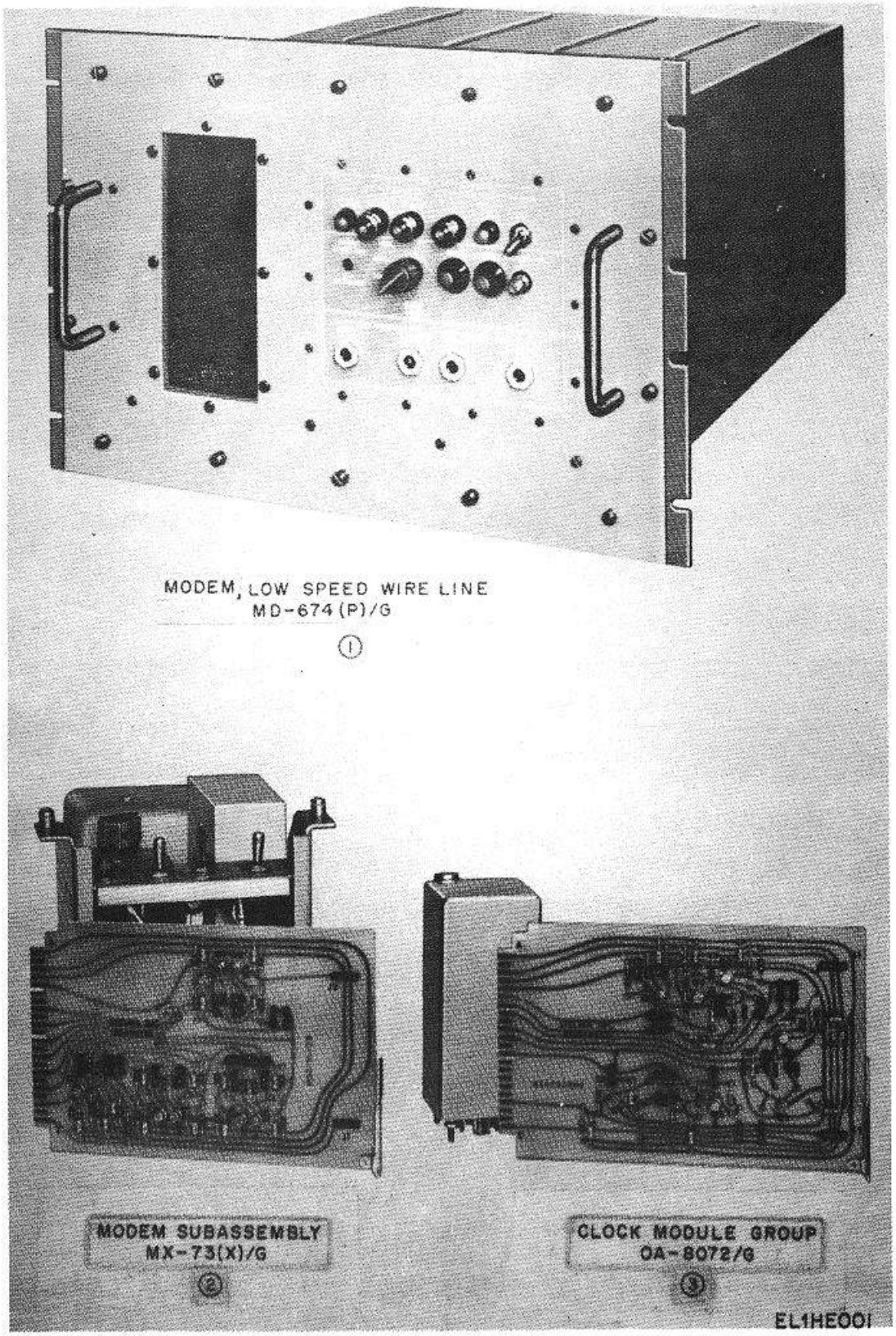


Figure 1-2. Modem, Low Speed Wire Line MD-674(P)/G, Modem Subassembly MX-73(*)/G, and Clock Module Group OA-8072/G.

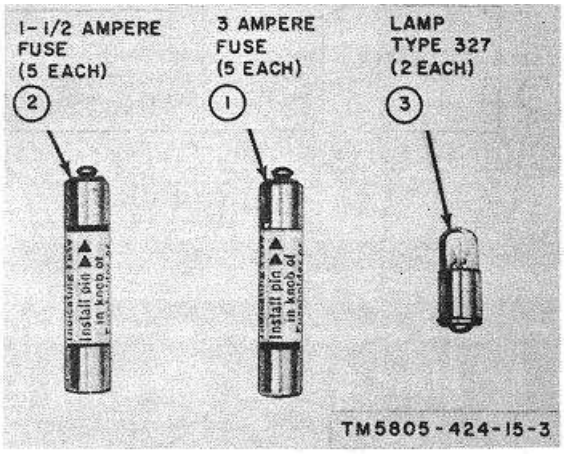


Figure 1-3. Running spares.

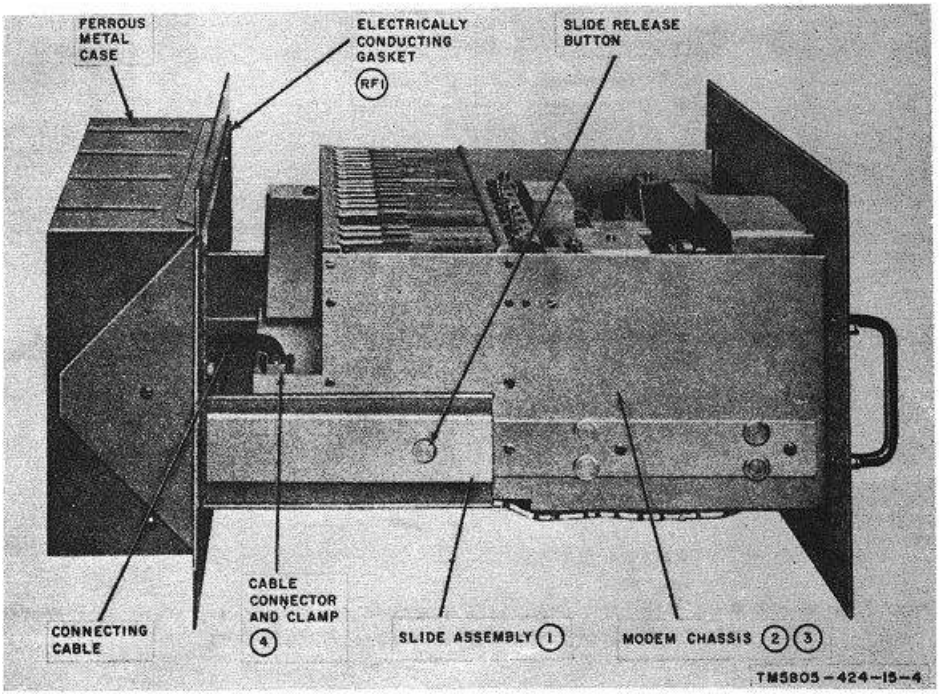


Figure 1-4. Modem, Low Speed Wire Line MD-674(P)/G, extended from case.

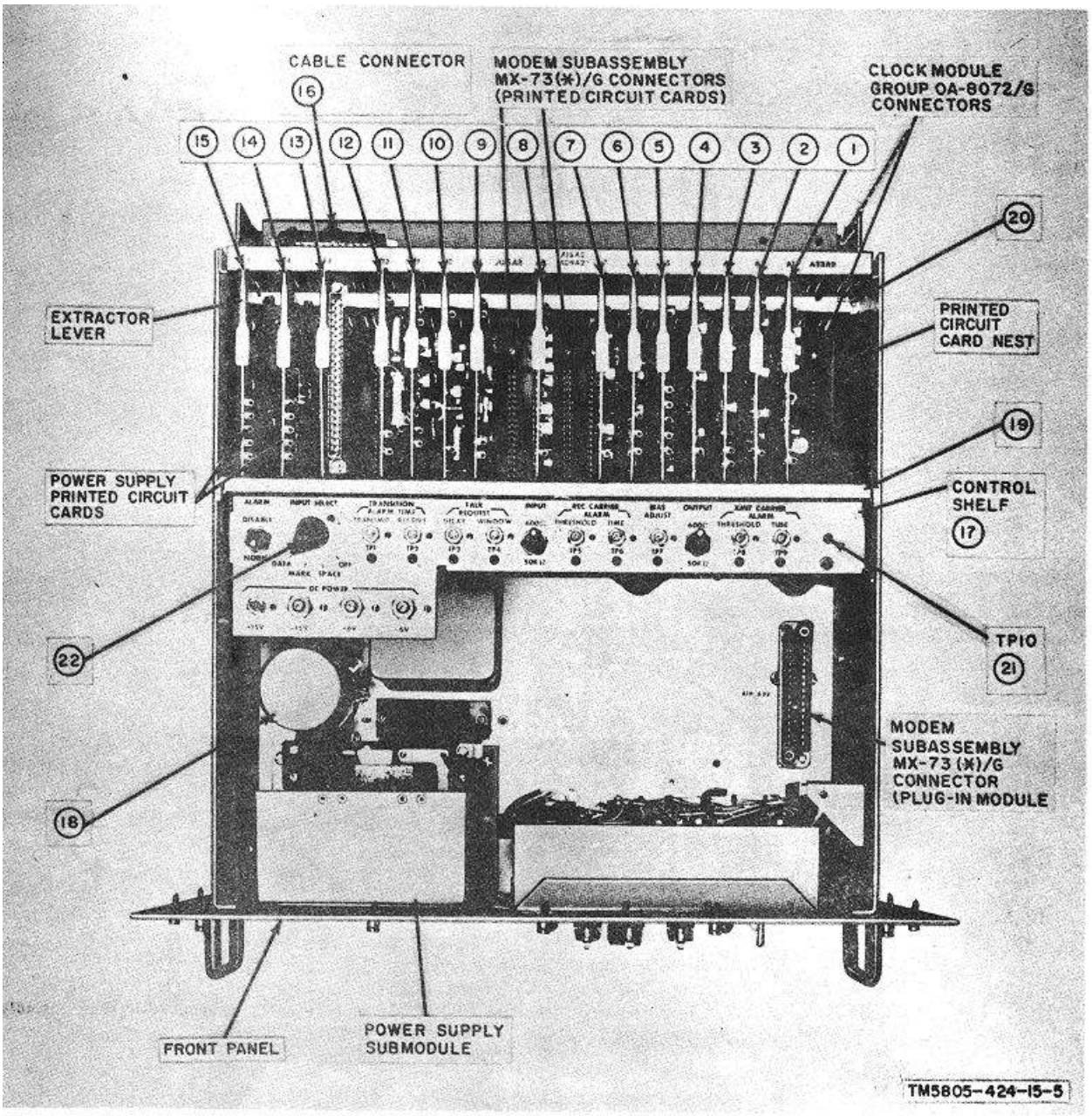


Figure 1-5. Modem, Low Speed Wire Line MD-674(P)/G, removed from case, top view, less Modem Subassembly MX-73(*)/G and Clock Module Group OA-8072/G.

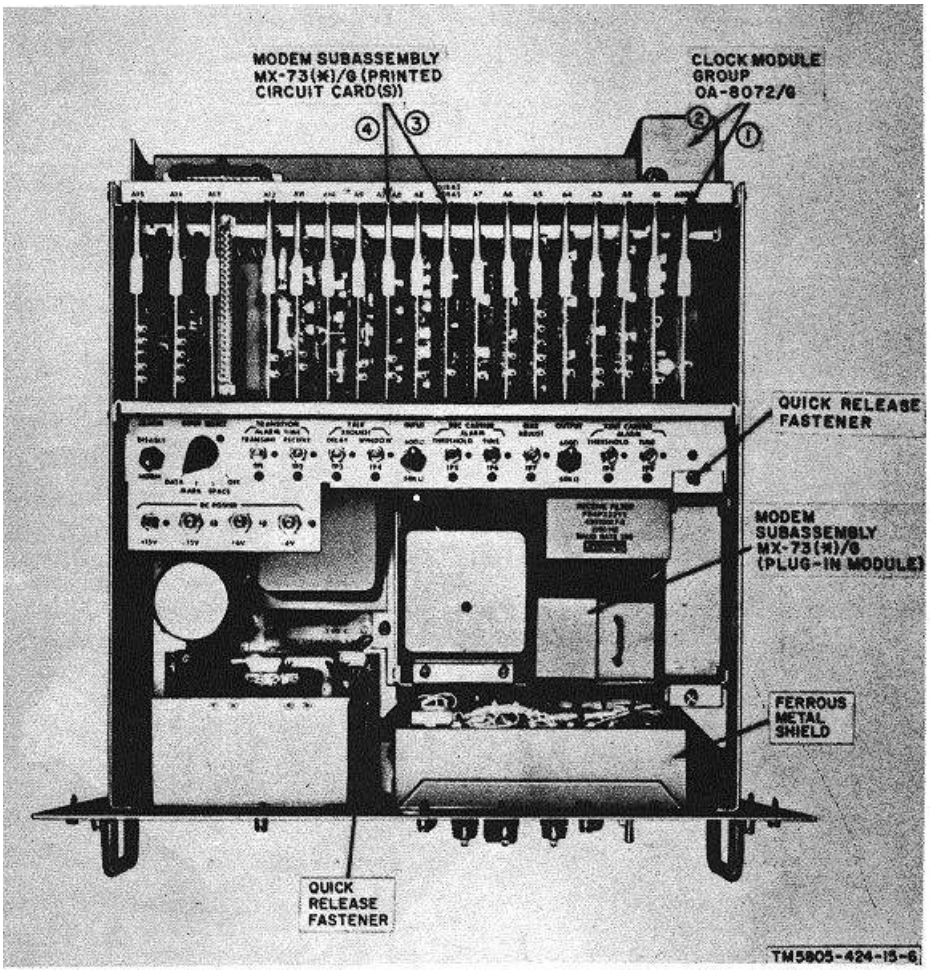


Figure 1-6. Modem, Low Speed Wire Line MD-74(P)/G removed from case, top view, with Modem Subassembly MX-73(*)/G and Clock Module Group OA-8072/G installed.

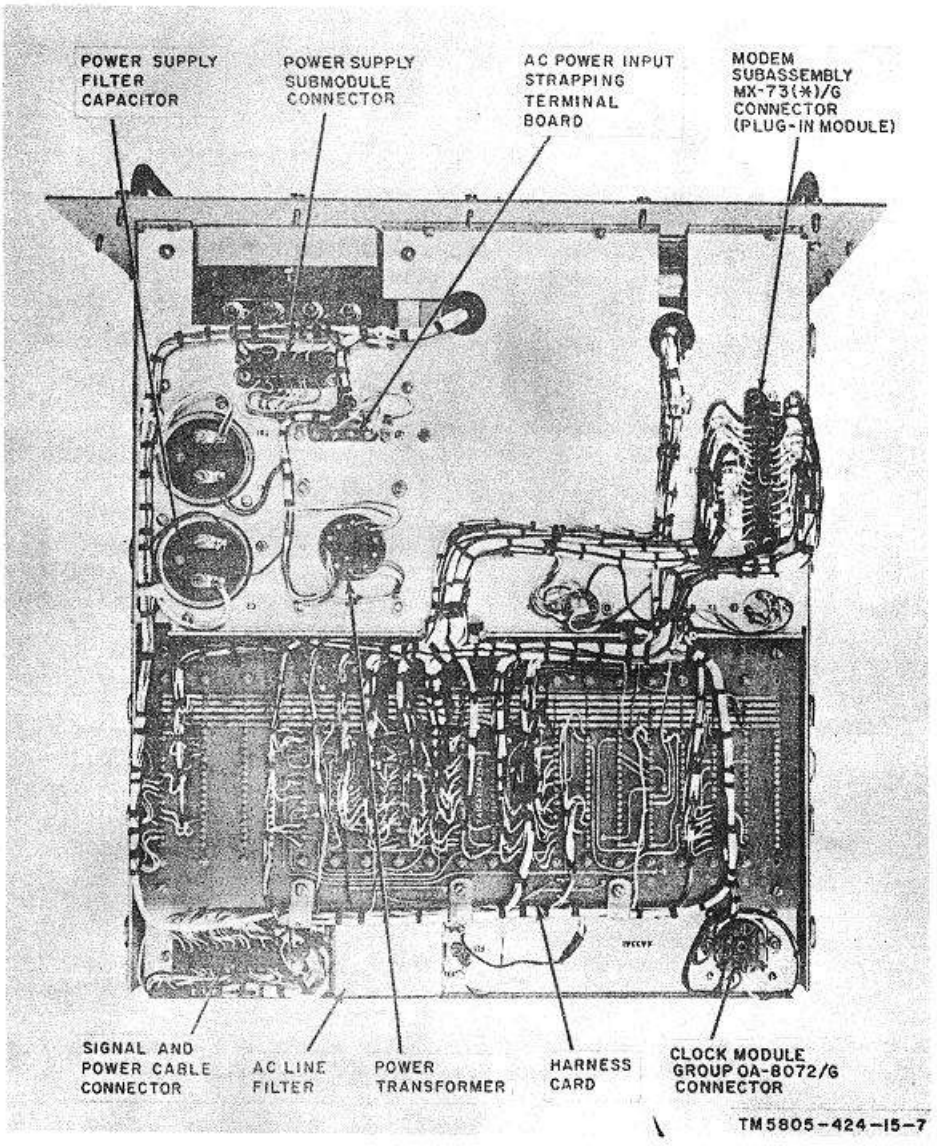


Figure 1-7. Modem , Low Speed Wire Line MD-674(P)/G removed from case, bottom view.

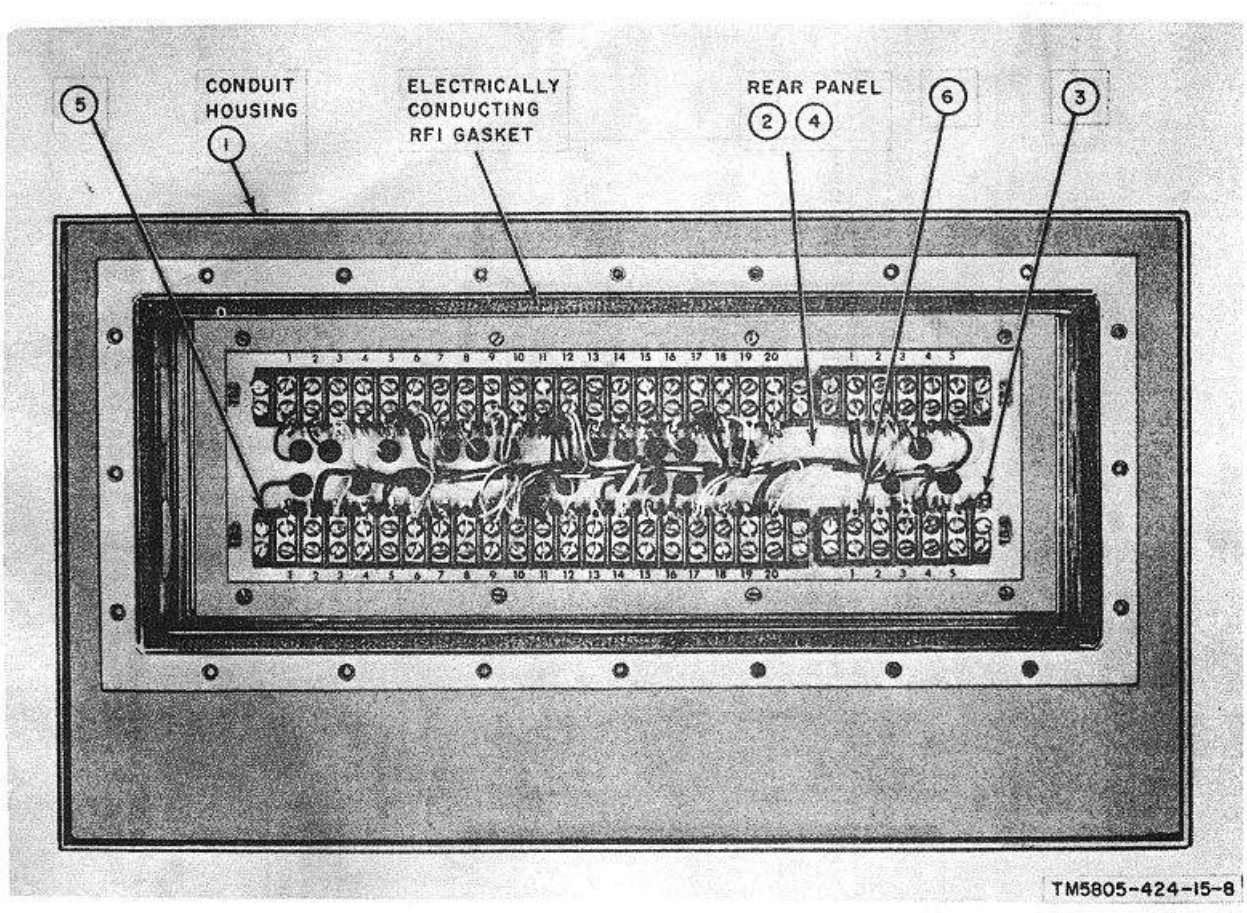


Figure 1-8. Modem, Low Speed Wire Line MD-674(P)/G, rear view, less access cover.

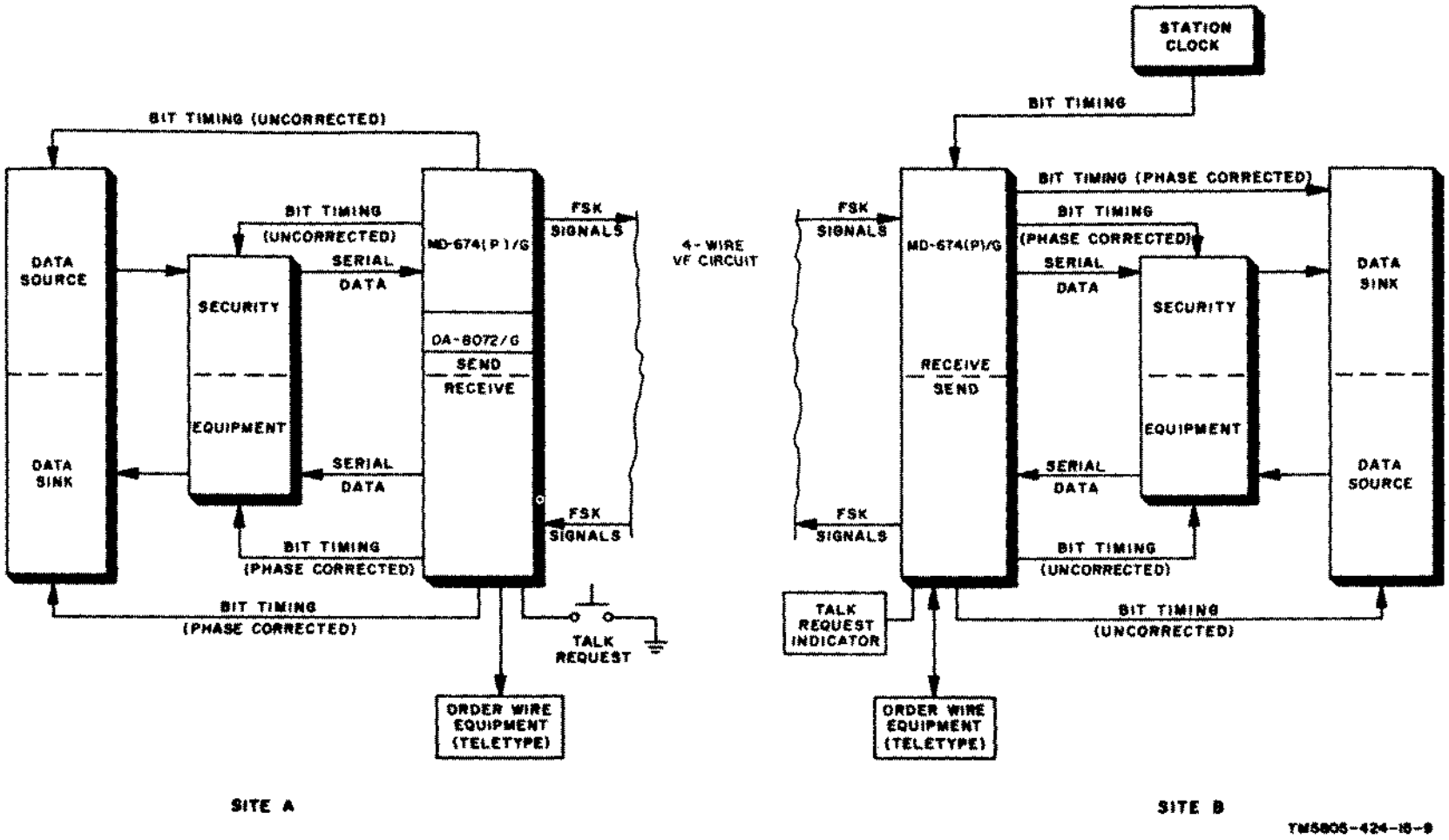


Figure 1-9. Single-channel, secure, terminal facilities, block diagram.

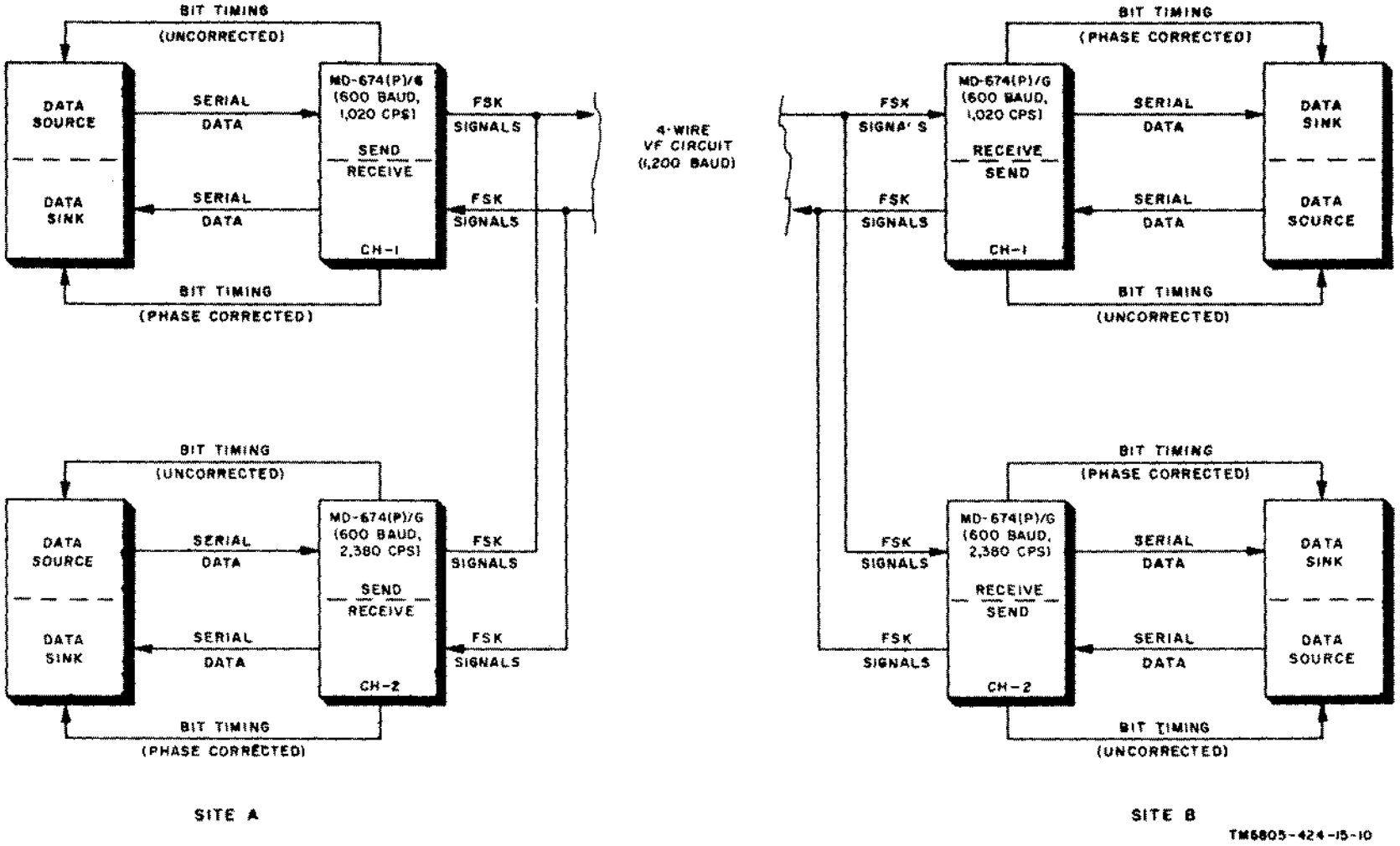


Figure 1-10. Multiplex terminal facilities, block diagram.

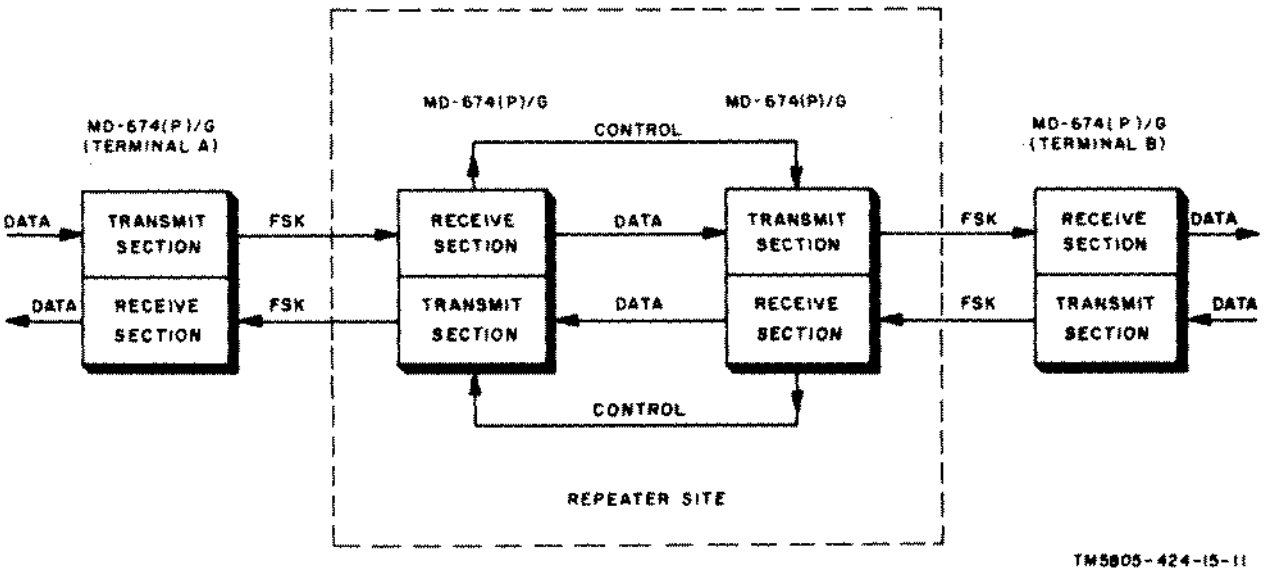


Figure 1-11. Signal-channel repeater facility, block diagram.

CHAPTER 2

INSTALLATION

Section I. SERVICE UPON RECEIPT OF EQUIPMENT

2-1. Unpacking

(fig. 2-1)

a. Packaging Data. When packed for domestic shipment, the MX-73(*)/G and the OA-8072/G are installed in the MD-674(P)/G. The MD-674(P)/G is placed in a waterproof, corrugated cardboard, inner carton and then inserted in a waterproof, corrugated cardboard, outer carton. For export shipment, the outer carton is packed in a wooden case. The wooden case is 17 1/2 inches high, 23 1/2 inches wide, and 28 3/4 inches long, and weighs approximately 85 pounds.

b. Unpacking. For domestic shipment, omit procedures given in (1) and (2) below.

(1) Cut and fold back the metal straps.

CAUTION

Do not attempt to pry off the wooden cover. Prying may damage the equipment.

(2) Remove the nails from the wooden cover and remove the wooden cover.

(3) Open the waterproof, corrugated cardboard, outer carton.

(4) Remove the spacers and pull out the waterproof, corrugated cardboard, inner carton.

(5) Open the corrugated cardboard, inner carton and remove the waterproof barrier bags which contain the spares and the technical manuals.

(6) Lift the MD-674(P)/G from the waterproof, corrugated cardboard, inner carton.

2-2. Checking Unpacked Equipment

a. Inspect the equipment for any loss or damage that might have occurred during shipment. If the equipment has been damage(d, or is incomplete, refer to procedures given in paragraph 1-3.

b. Check the equipment against the packing list.

c. If the equipment has been used or reconditioned, check to see if is has been changed by a modification work order (MWO). If the equipment has been modified, the MWO number will appear on the front panel near the nomenclature.

Section II. INSTALLATION

2-3. Installation Procedures

The MD-674(P)/G may be installed in a standard, 19-inch relay rack. It requires 12 13/16 inches of vertical rack space. Install the MD-674(P)/G in a relay rack as follows:

CAUTION

Do not install the MD-674(P)/G directly above, below, or adjacent to equipment which generates excessive heat. Excessive heat will damage the transistors.

a. Unscrew the screws that secure the front panel to the outer case, and slide the chassis forward until the slide stops are reached.

b. Disengage the cable connector at the rear of the chassis (fig. 1-4).

c. Depress the slide release button on each side of the chassis and pull the chassis out of the case.

d. Position the case in the relay rack and secure the case to the relay rack with a panel bolt in each retaining slot of the mounting flange (fig. 1-1).

e. Position the chassis in the case and slide it back until the slide stops engage.

CAUTION

A radio frequency interference (rfi) gasket is used in the front panel to prevent signal

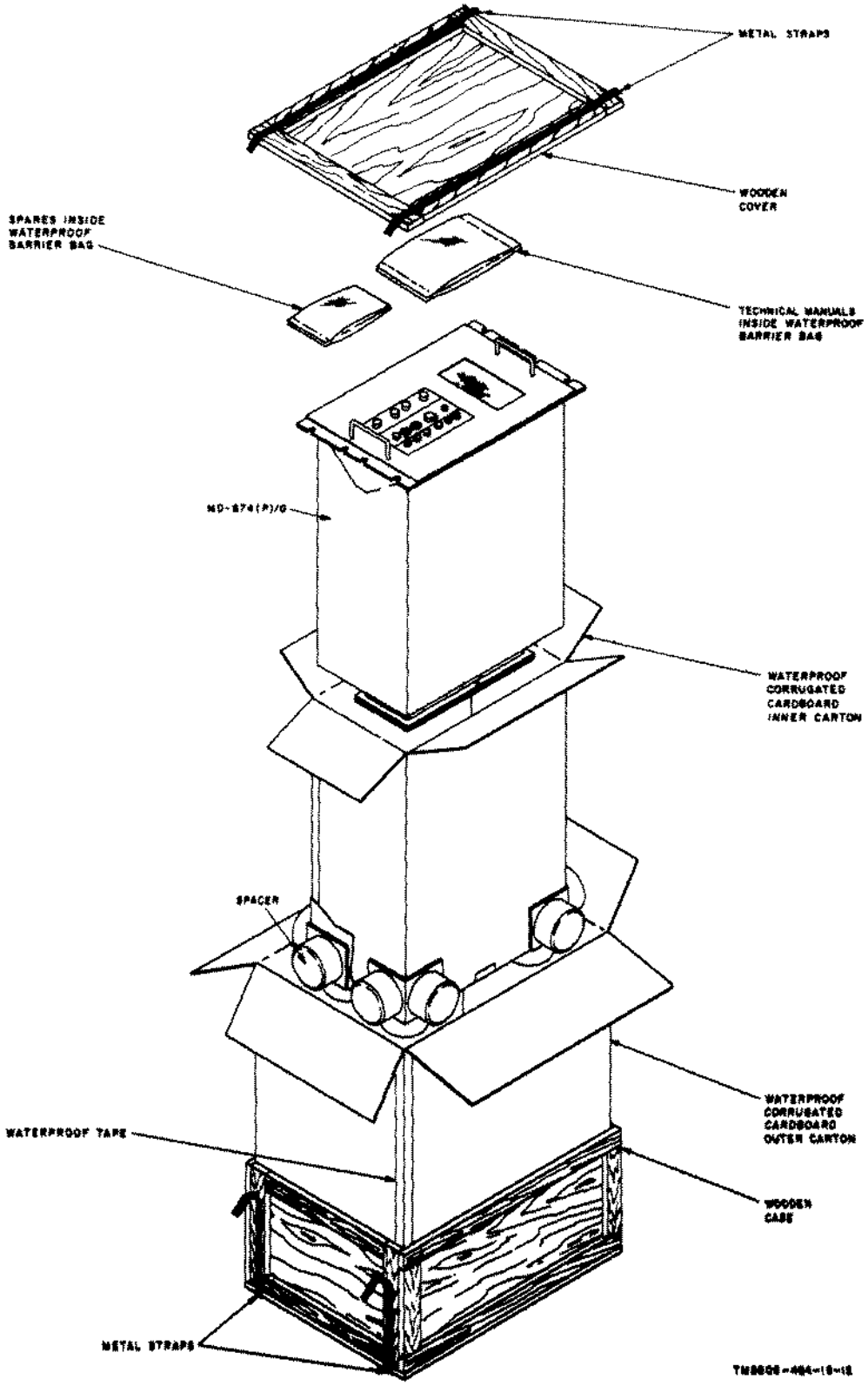


Figure 2-1. Typical packaging diagram.

radiation. Be careful not to damage the rfi gasket when securing the chassis to the case.

f. Connect the cable connector on the rear of the chassis; slide the chassis completely into the case, and secure the chassis to the case with the front panel securing screws.

2-4. Strapping Options

a. AC Power. Determine the type of alternating current (ac) power to be used and be sure that only the required strapping ((1) or (2) below) is used.

(1) *115 volts*. Connect a strap between terminals 1 and 2, and terminals 3 and 4 on the ac power input strapping terminal board (fig. 1-7).

(2) *230 volts*. Connect a strap between terminals 2 and 3 of the ac power input strapping terminal board (fig. 1-7).

b. Station Clock Signal.

(1) *Internal*. Strap terminals TP3 and TP4 on assembly A1 (A, fig. 2-5).

(2) *External*. Strap terminals TP1 to TP2 and TP4 to TP5 on assembly A1 (A, fig. 2-5).

c. Received Data Output Signal.

(1) *Retimed.*

(*a*) Strap terminals 1 and 3 on the harness card (fig. 2-4).

(*b*) Strap terminals 3 and 4 on assembly A11 (B, fig. 2-5).

(2) *Not retimed*.

(*a*) Strap terminals 2 and 3 on the harness card (fig. 2-4).

(*b*) Strap terminals 2 and 4 on assembly A11 (B, fig. 2-5).

d. Order Wire Signal. If the order-wire facility is to be used, strap terminals 1 and 4 on assembly A11 (B, fig. 2-5); then select either option provided below:

(1) *Terminal applications*. The manual reset option may be used at both MD-674(P)/G's in the link, but only one of the MD-674(P)/G's may use the automatic reset option

(*a*) *Manual reset*. Strap terminals 5 and 6 on the harness card (fig. 2-4).

(*b*) *Automatic reset*. Strap terminals 4 and 6 on the harness card (fig. 2-4).

(2) *Repeater applications*. Each MD-674(P)/G may be strapped as described in (1) above when an operator is stationed at the site. When no operator is stationed at the site, make the strapping connections indicated below.

(*a*) Strap terminals 1, 2, and 3 on assembly A3 (C, fig. 2-5).

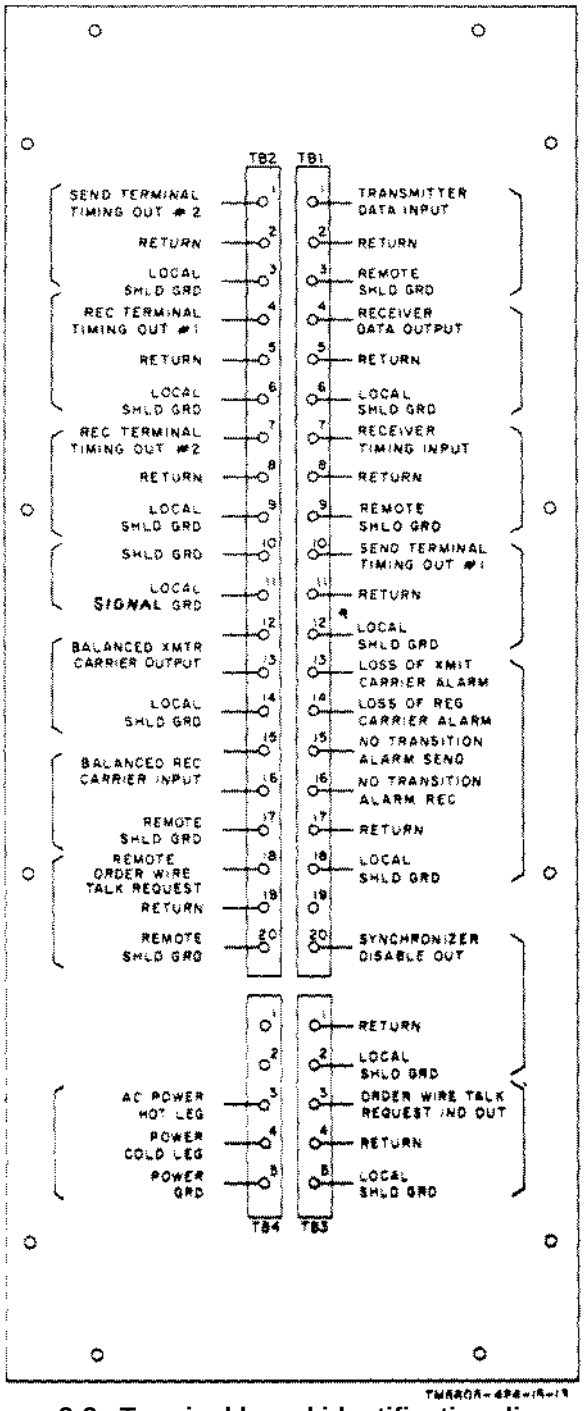


Figure 2-2. Terminal board identification diagram.

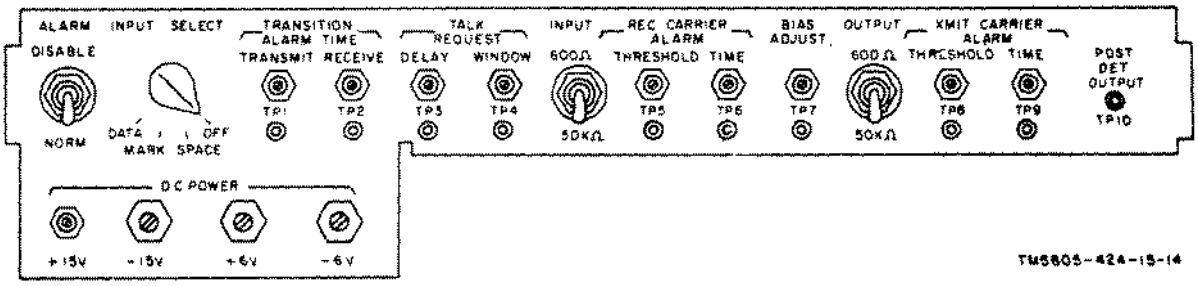


Figure 2-3. Control shelf, controls and test jacks.

(*b*) Strap terminals 1 and 2 on assembly A10 (D, fig. 2-5).

e. Synchronization or Common Alarm.

(1) *Signal*. To provide an external synchronize disable signal at terminal 20 of terminal board TB1, strap terminals 1 and 2 on assembly A12 (E, fig. 2-5).

(2) *Common Alarm*. To provide an external common alarm at terminal 20 of terminal board TB1, strap terminals 2 and 3 on assembly A12 (E, fig. 2-5).

f. Negative Mark Input. Each MX-73(*)/G is strapped to receive positive mark signal (terminals 13 and 14 of connector P1, fig. 6-43, 6-44, or 6-45). If the MD-674(P)/G is to be used to receive a negative mark signal, remove the strap from terminals 13 and 14 of connector P1 on the MX-73(*)/G and reconnect the strap between terminals 14 and 15.

2-4.1. Coordination of Components

For operation at the various frequencies the components to be installed are matched in accordance with the following table, and paragraph 1-6.

Modem subassembly	*Frequency determining divider*	*Card assembly*
MX-7372/G	D80034200 (8)	A18A2-A19A2
MX-7373/G	D80034200 (8)	A18A2-A19A2
MX-7374/G	D80034190 (4)	A20A2-A22A2
MX-7375/G	D80034190 (4)	A20A2-A22A2
MX-7376/G	D80034190 (4)	A20A2-A22A2
MX-7377/G	D80034180 (2)	A23A2-A29A2
MX-7378/G	D80034180 (2)	A23A2-A29A2
MX-7379/G	D80034180 (2)	A23A2-A29A2
MX-7380/G	D80034180 (2)	A23A2-A29A2
MX-7381/G	D80034180 (2)	A23A2-A29A2
MX-7382/G	D80034180 (2)	A23A2-A29A2
MX-7383/G	D80034180 (2)	A23A2-A29A2
MX-7384/G	None.	
MX-7385/G	None.	
MX-7386/G	None.	

NOTE

No frequency divider circuit card is inserted in the A18A2-A29A2 slot when Modem subassembly MX-7384, or MX-7385, or MX-7386 is installed. When these subassemblies are used a strap must be connected from pin 19 to pin 20 of P1 of the module. (This is to bridge the circuit gap which results when the A18A2-A29A2 slot is vacant.)

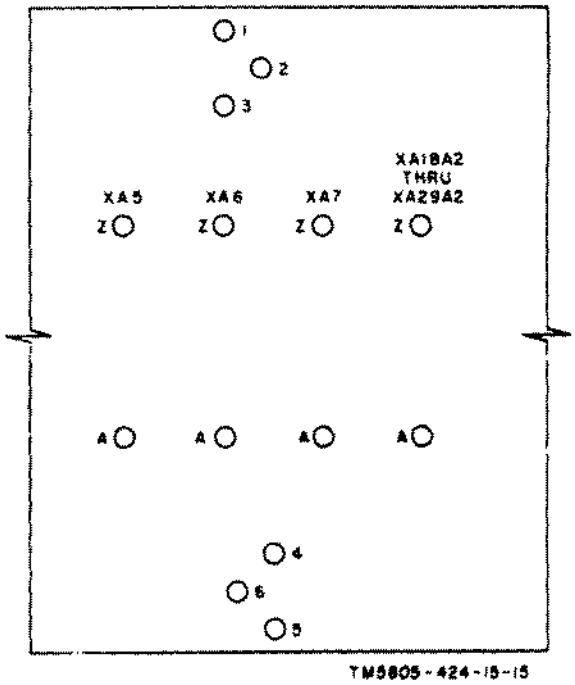


Figure 2-4. Harness card strap terminal locations.

2-5. Connections

a. General. All signal and power connections to the MD-674(P)/G are made to the terminal boards on the rear of the chassis when the access cover is removed (fig. 1-8). Determine the installation requirements and the number of cable runs to be used, and punch out the required holes with a Greenly punch. Determine the type of wiring required from the chart below, and connect the equipment as required in *b, c*, or *d* below.

Type	*Connection*
Shielded twisted pair, Alpha No. 3241 to MIL-W - 168780.	Transmitter data input. External bit-timing input. Receive data output. All bit-timing outputs. All order-wire connections. AC power
Shielded twisted pair, Alpha No. 3221 to MIL-W-168780.	Transmitter carrier output. Receiver carrier input.
Shielded wire, Alpha No. 1375 MIL-W-76B.	All ground connections.
Shielded wire, Alpha No. 3308 to MIL-W-16878D.	All external alarm connections.

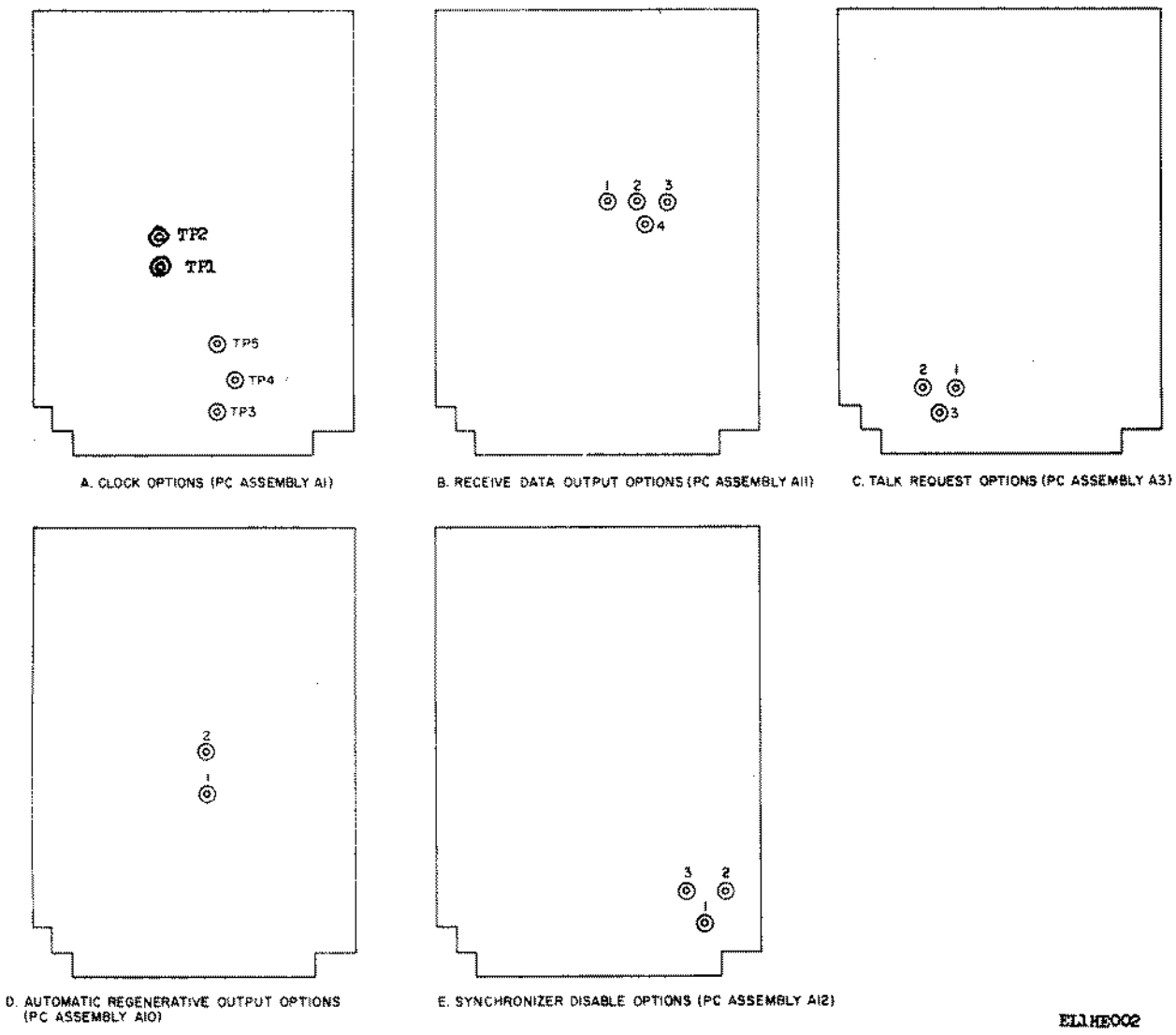


Figure 2-5. Printed-circuit card assembly strap terminal locations.

b. Single-Channel Terminal Connections (fig. 2-2).

(1) Connect the 115- or 230-volt ac power to terminals 3,4, and 5 of terminal board TB4.

(2) Connect the digital input (to be transmitted to terminals 1, 2, and 3 of terminal board TB1.

Note. **The digital input return line should be returned to a signal ground at the signal source end. If it is not, connect the return line (terminal 2 of TB1) to the signal ground at terminal 11 of terminal board TB2 of the MD-674(P)/G.**

(3) Connect the uncorrected timing signal from terminals 1,2,and 3 of terminal board TB2 to the digital data transmit equipment.

Note. **If security equipment is used (fig. 1-9), connect the uncorrected timing signal from terminals 10, 11, and 12 of terminal board TB1 to the security transmit equipment.**

(4) Connect the digital output (received) from terminals 4, 5, and 6 of terminal board TB1 to the digital data receive equipment.

(5) Connect the corrected timing signal from terminals 4, 5, and 6 of terminal board TB2 to the digital data receive equipment.

Note. **If security equipment is used (fig. 1-9), connect the corrected timing signal from terminals 7, 8, and 9 on terminal board TB2 to the security receive equipment.**

(6) If the station clock signal is generated by another equipment, connect the station clock signal to terminals 7, 8, and 9 of terminal board TB1.

Note. **The external clock signal return line should be returned to a signal ground at the signal source end. If it is not, connect the return line (terminal 8 of TB1) to the signal ground at terminal 11 of terminal board TB2 of the MD674(P)/G.**

(7) If external alarm indicators are required, connect the alarm output from terminals 13 through 18 of terminal board TB1 to the alarm indicators.

(8) If an external order-wire control (in place of TALK REQUEST pushbutton) is to be used, connect the circuit to terminals 18, 19, and 20 of terminal board TB2.

(9) If an external order-wire control indicator is to be used, connect the output from terminals 3, 4, and 5 of terminal board TB3 to the order-wire control indicator.

(10) To disable the digital data receive equipment when the carrier signal (vf receive) fails, connect terminal 20 of terminal board TB1, and terminals 1 and 2 of terminal board TB3, to the disable (inhibit) circuit of the digital data receive equipment.

(11) Connect the vf output (send side) from terminals 12, 13, and 14 of terminal board TB2.

(12) Connect the vf input (receive side) to terminals 15, 16, and 17 of terminal board TB2.

(13) Connect the ground leads to a centralized grounding point as follows:

Note. **Normally, shield grounds are connected at the signal driving end of the connecting wires. The designations LOCAL SHLD ORD and REMOTE SHLD GRD, at each individual input and output line, indicate which end of the shield should be grounded. Do not ground the shield at both ends of the line. Each individual ground bus must be connected to the centralized grounding point through separate ground leads.**

(a) Remote.

1. Connect the common shield ground at terminal 10 of terminal board TB2 to the centralized grounding point.

2. Connect the common signal ground at terminal 11 of terminal board TB2, through a separate wire, to the centralized grounding point.

3. Connect the case (ac) ground at terminal 5 of terminal board TB4, through a separate wire, to the centralized grounding point.

(b) Local. If all the shield grounding (including those recommended for remote grounding) and signal grounding is to be made at the MD-674(P)/G, connect a ground lead between terminal 10 of terminal board TB2 and terminal 5 of terminal board TB4 and a separate ground lead between terminal 11 of terminal board TB2 and terminal 5 of terminal board TB4.

c. Multiplex Terminal Connection.

(1) Connect one of the MD-674(P)/G's as indicated in *b*(1) through (13) above.

(2) Connect the remaining MD-674(P)/G's as indicated in *b*(1) through (10) and (13) above.

(3) Connect parallel connections between terminals 12, 13, and 14 of terminal board TB2 on each MD-674(P)/ G.

(4) Connect parallel connections between terminals 15, 16, and 17 of terminal board TB2 on each MD-674(P)/G.

(5) Operate the INPUT and OUTPUT impedance switches (fig. 2-3) on one of the MD-674(P)/G's to 600Ω.

(6) Operate the INPUT and OUTPUT impedance switches on the remaining MD674(P)/G's to 50KΩ.

d. Single-Channel Repeater Connection.

(1) Connect the 115- or 230-volt ac power to terminals 3, 4, and 5 of terminal board TB4 on both MD-674(P)/G's.

(2) Connect terminals 1, 2, and 3 of terminal board TB1 on each MD-674(P)/G to terminals 4, 5, and 6 of terminal board TB1 on the opposite MD-674(P)/G.

(3) If neither MD-674(P)/G contains an OA-8072/G, connect external timing signals to terminals 7, 8, and 9 of terminal board TB1 on each MD-674(P)/G. If only one MD-674(P)/G contains an OA-8072/G, connect terminals 10, 11, and 12 of TB1 on the MD-674(P)/G with the OA-8072/G to terminals 7, 8, and 9, respectively, of terminal board TB1 on the MD-674(P)/G without the OA-8072/G. If both units contain an OA-8072/G, remove the OA-8072/G from one unit, strap for external clock (para 2-4*b*), and connect timing in accordance with preceding sentence.

(4) Connect the vf output (send side) from terminals 12, 13, and 14 of terminal board TB2.

(5) Connect the vf input (receive side) to terminals 15, 16, and 17of terminal board TB2.

(6) Connect terminals 3, 4, and 5 of terminal board TB3 on each MD-674(P)/G to terminals 18, 19, and 20 of terminal board TB2 on the opposite BD-674(P)/G.

(7) Connect the ground leads as indicated in *b*(13) above.

(8) Operate the INPUT and OUTPUT impedance switches (fig. 2-3) on both of the MD674(P)/G's to 6000.

Section III. INITIAL ADJUSTMENTS

NOTE

The procedures given below are performed by general support maintenance personnel, or equivalent.

2-6. Test Equipment Required

a. Multimeter ME-26A/U.

b. Oscilloscope, Hewlett-Packard Model 140A.

c. Voltmeter, Electronic ME-30A/U.

d. Attenuator, Hewlett-Packard Model 350D.

e. Temperature tester (Simpson Model 388-3L).

2-7. Loop-Back Adjustments

a. Preliminary Procedures.

(1) Tag and disconnect leads from terminals 12, 13, and 14 and terminals 15, 16, and 17 of terminal board TB2.

(2) Use a shielded twisted pair signal cable and connect terminals 12, 13, and 14 to terminals 15, 16, and 17 of terminal board TB2, respectively.

(3) Tag and disconnect leads from terminals 3, 4, and 5 of terminal board TB3, and terminals 18, 19, and 20 of terminal board TB2.

(4) Use a shielded twisted pair signal cable and connect terminals 3, 4, and 5 of terminal board TB3 to terminals 18, 19, and 20 of terminal board TB2, respectively.

(5) Operate the BAUD RATE switch to the required position (fig. 3-1).

(6) Operate the AC POWER switch to ON.

b. Power Supply Adjustments.

(1) Connect the ME-26A/U, set to measure 15 volts dc, between jacks J2 (+15 volts) and J5 (ground) on assembly A15 (left power supply printed-circuit card, fig. 1-5).

(2) Adjust the D.C. POWER +15V control (fig. 2-3) until the ME-26A/U indicates 15 volts dc; then, disconnect the ME-26A/U.

(3) Connect the ME-26A/U, set to measure -15 volts dc, between jacks J4 (-15 volts) and J5 (ground) on assembly A15 (fig. 1-5).

(4) Adjust the D.C. POWER -15V control (fig. 2-3) until the ME-26A/U indicates -15 volts dc; then, disconnect the ME-26A/U.

(5) Connect the ME-26A/U, set to measure 6 volts dc, between test jacks J2 (+6 volts) and J5 (ground) on assembly A14 (right power supply printed circuit card) (fig. 1-5).

16) Adjust the D.C. POWER +6V control (fig. 2-3) until the ME-26A/U indicates 6 volts dc; then, disconnect the ME-26A/U.

(7) Connect the ME-26A/U. set to measure -6 volts dc, between test jacks J4 (-6 volts) and J5 (ground) on assembly A14 (fig. 1-5).

(8) Adjust the D.C. POWER -6V control (fig. 2-3) until the ME-26A/U indicates -6 volts dc; then, disconnect the ME-26A/U.

c. Transmit Output Level Adjustments.

(1) Connect the ME-30A/U across terminals 12 and 13 of terminal board TB2 (fig. 2-2).

(2) Operate the INPUT SELECT switch (fig. 2-3) to DATA.

(3) Operate the digital data transmitting equipment.

(4) Adjust the OUTPUT LEVEL ADJ control (fig. 3-1) until the ME-30A/U indicates the desired output level (between +3 decibels (referred to 1 milliwatt in 600 ohms) (dBm) and -20 (dBm)).

(5) Disconnect the ME-30A/U.

d. Alarm Adjustments.

(1) Connect the oscilloscope between jack J3 of assembly A12 (fig. 1-5) and ground.

(2) Operate the oscilloscope to observe a 5second pulse.

(3) Operate the INPUT SELECT switch (fig. 2-3) to OFF. Adjust the TRANSITION ALARM TIME TRANSMIT control to obtain a ground level indication on the oscilloscope 5 seconds ±5 percent after the INPUT SELECT switch is operated; then, disconnect the oscilloscope.

(4) Connect the oscilloscope between jack J4 on assembly A11 (fig. 1-5) and ground.

(5) Operate the INPUT SELECT switch (fig. 2-3) to OFF. Adjust the TRANSITION ALARM TIME RECEIVE control to obtain a ground level indication on the oscilloscope 5 seconds ±5 percent after the INPUT SELECT switch is operated; then, disconnect the oscilloscope.

(6) Connect the ME-30A/U across terminals 12 and 13 of terminal board TB2 (fig. 2-2).

(7) Connect the oscilloscope (set to observe a 2-second pulse) between jack J4 on assembly A6 (fig. 1-5) and ground.

(8) Adjust the OUTPUT LEVEL ADJ control (fig. 3-1) until the ME-30A/U indicates 10 decibels (dB) below the desired output level (*c* above).

(9) Adjust the XMIT ALARM THRESHOLD control (fig. 2-3) until the oscilloscope indicates a continuous ground level; then, slowly reverse the adjustment direction until the oscilloscope indicates a positive level.

(10) Adjust the OUTPUT LEVEL ADJ control (fig. 3-1) for the desired output level on the ME-30A/U; the oscilloscope will indicate a positive level.

(11) Adjust the OUTPUT LEVEL ADJ control (fig. 3-1) until the ME-30A/U indicates 10 dB below the desired output level. Adjust the XMIT CARRIER ALARM TIME control (fig. 2-3) to obtain a ground level indication on the oscilloscope 2 seconds after the OUTPUT LEVEL ADJ control is operated.

(12) Adjust the OUTPUT LEVEL ADJ control until the ME-30A/U indicates the desired output level; then, disconnect the ME-30A/U and the oscilloscope.

(13) Connect the attentuator between terminals 12 and 15 of terminal board TB2 (fig. 2-2).

(14) Connect the ME-30A/U to terminals 15 and 16 of terminal board TB2.

(15) Connect the oscilloscope (set to observe a 2-second pulse) between jack J4 on assembly A9 (fig. 1-5) and ground.

(16) Adjust the attenuator until the ME30A/U indicates the desired receive carrier level.

(17) Adjust the attenuator until the ME30A/U indicates 20 dB less than the desired receive carrier level.

(18) Adjust the REC CARRIER ALARM THRESHOLD control (fig. 2-3) until the oscilloscope indicates a continuous +6-volt level; then, slowly reverse the adjustment direction until the oscilloscope indicates a -6 volt level.

(19) Adjust the attenuator for the desired receive carrier level; the oscilloscope will indicate -6 volts dc.

(20) Adjust the attenuator until the ME30A/U indicates 20 dB less than the desired receive carrier level. Adjust the REC CARRIER ALARM TIME control (fig. 2-3) to obtain a -6volt dc level on the oscilloscope 2 seconds after the attenuator is operated.

e. Oven Temperature Adjustments.

(1) *General.* Oven temperature has been pre-set at the factory or depot and R1 (figs. 2-6, 2-7 or 2-8) is locked and staked with varnish. Readjustment should normally not be required. When temperature reading or readjustment is considered necessary it should be performed only in accordance with procedure provided in (2) below.

CAUTION

Setting of R1 should not be changed unless done in accordance with procedure. Adjustment of R1 without use of proper temperature indicator can result in high oven temperature, which will seriously damage or destroy components within the oven assembly.

(2) *Adjustment.*

(*a*) Remove screw in top of oscillator and oven assembly and insert thermocouple probe of temperature tester (Simpson Model 388-3L), NSN 6685-00-975-4544, into oven through screw hole.

(*b*) Observe oven temperature until a stable reading is obtained. If not 75°C proceed to (*c*) below.

(*c*) Adjust OVEN TEMP ADJUST control R1 over a period of 10 minutes to obtain a 75°C indication on the temperature tester. Lock setting of R1 and apply a drop of glyptal varnish to shaft.

(*d*) Remove probe from oven and replace screw.

f. Final Procedure.

(1) Disconnect the test equipment and the shielded twisted pair signal cable connected in *a* above.

(2) Connect the tagged leads disconnected in *a* above to the terminal boards.

2-8. System Adjustments

a. Bias.

(1) Connect the oscilloscope between test point TP7 on the control shelf (fig. 2-3) and ground.

(2) Adjust the oscilloscope to observe two crossover patterns.

(3) Adjust the BIAS ADJ control for minimum distortion (crossover points as near the center of the pattern as possible); then, disconnect the oscilloscope.

b. Delay Equalization (MX-7373/G, MX-7375/G, MX-7383/G, and MX-7385/G).

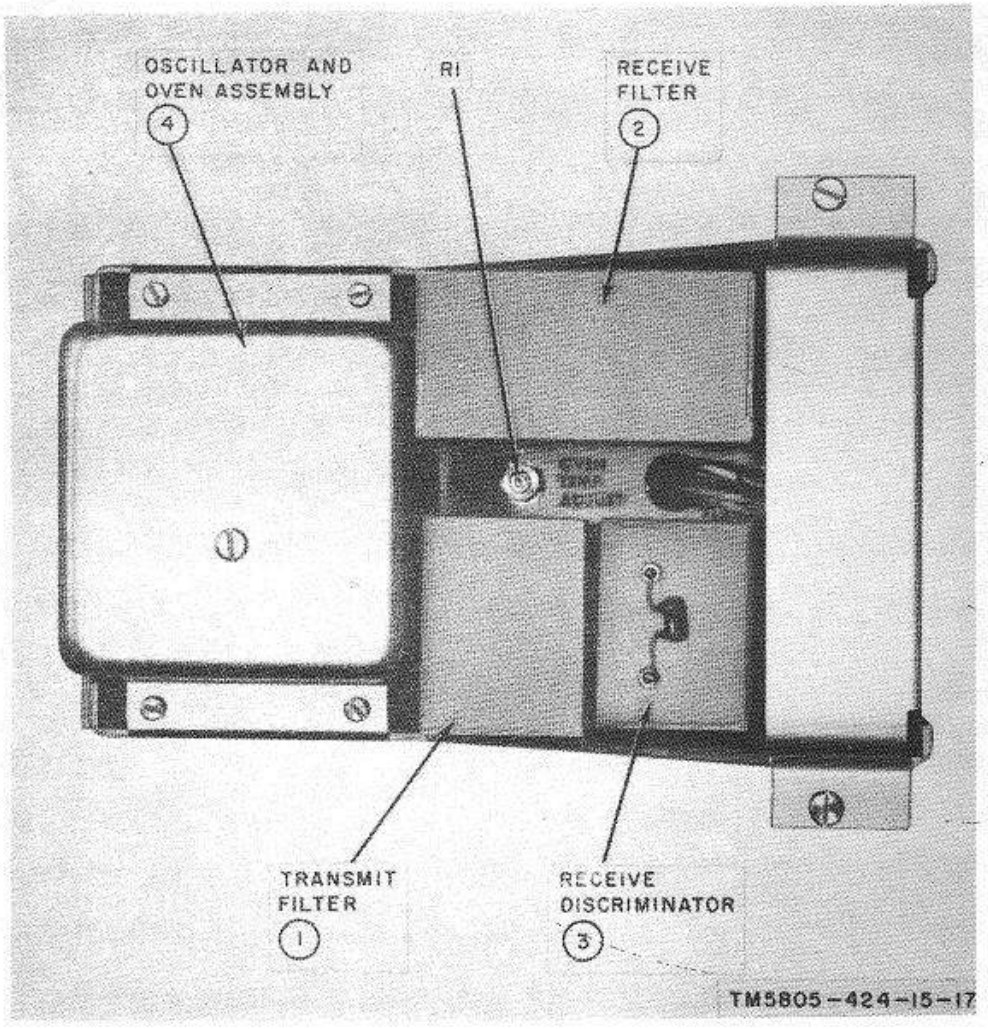


Figure 2 6. Plug-in module of Modem Subassembly MX-7372/G, MX-7374/G, MX-7376/G, MX-7377/G, MX-7378/G, MX-7380/G MX-7381/G, MX-7382/G, MX 7384/G, or MX-7386/G.

(1)Connect the oscilloscope between test point TP10 on the control shelf (fig. 2-3) and ground, and adjust the oscilloscope to observe at least two eye-patterns.

(2) Rotate the EQUALIZER switch (fig. 2-7) to the position that provides a maximum opening of the eye-pattern; then, disconnect the oscilloscope.

c. Delay Equalization (MX-7379/G).

(1) *Selectable.*

(*a*) Connect the oscilloscope between test point TP10 on the control shelf (fig. 2-3) and ground, and adjust the oscilloscope to observe at least two eye-patterns.

(*b*) Operate the EQUALIZER switch (fig. 2-8) to COMP.

(*c*) Operate the EQ1 and EQ2 FREQ switches to each of their positions, in various combinations, until a maximum opening is obtained in the eye-pattern without distortion.

(*d*) If delay equalization cannot be achieved without introducing distortion, operate the EQUALIZER switch to OUT.

(2) *Adjustable.*

(*a*) Connect the oscilloscope between test point TP10 on the control shelf (fig. 2-3) and ground, and adjust the oscilloscope to obtain at least two eye-patterns.

(*b*) Operate the EQUALIZER switch (fig. 2-8) to ADJ, and both FREQ switches to A.

(*c*) Adjust the EQ1 DELAY ADJ control to obtain a maximum opening in the eye-pattern without distortion; note the pattern.

(*d*) Adjust the EQ2 DELAY ADJ control to obtain a maximum opening in the eye-pattern without distortion; note the pattern.

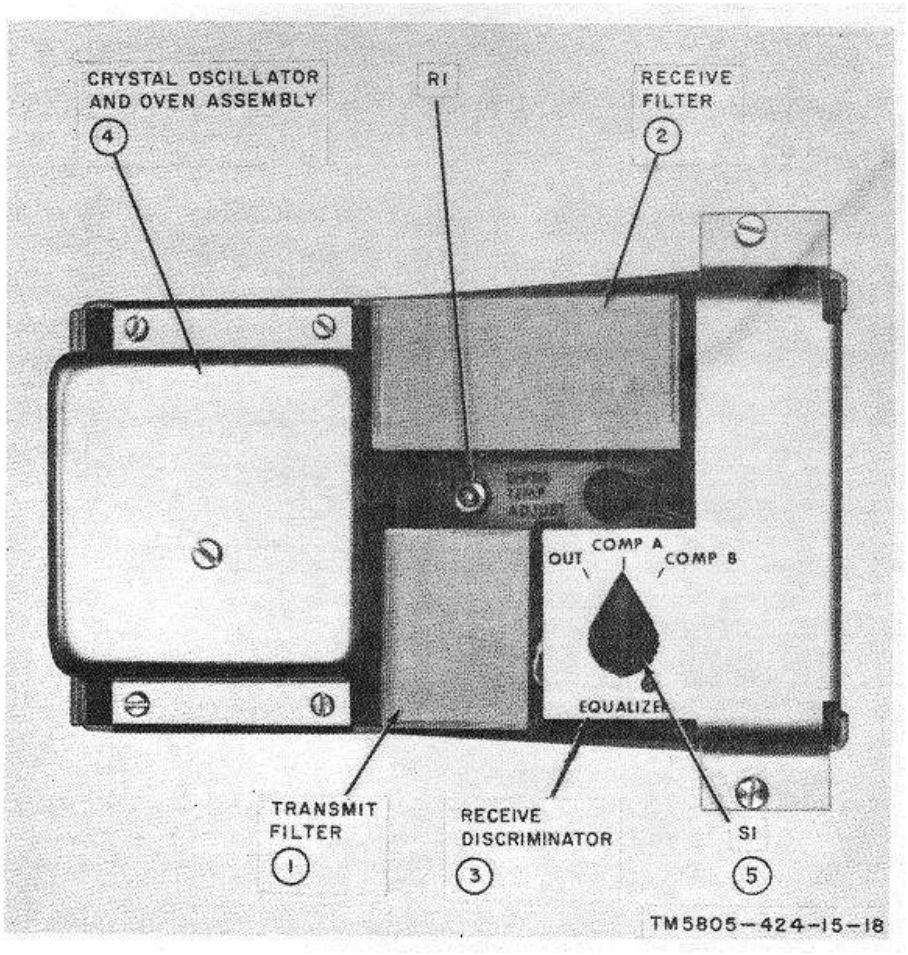


Figure 2-7. Plug-in module of Modem Subassembly MX-7373/G, MX-7375/G, MX-7383/G, or MX-7385/G.

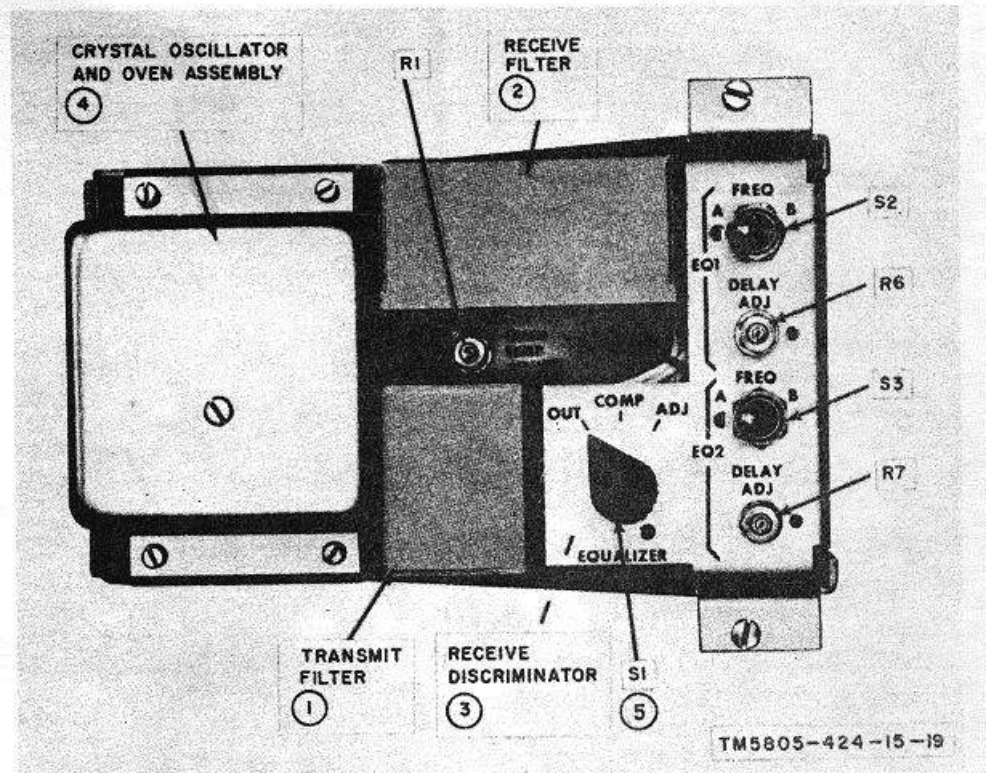


Figure 2-8. Plug-in module of Modem Subassembly MX-7379/G.

(*e*) Operate the EQ1 FREQ switch to B and repeat the procedures given in (*c*) and (*d*) above; note the pattern.

(*f*) Operate the EQI FREQ switch to the position that provides the best pattern.

(*g*) Operate the EQ2 FREQ switch to B and repeat the procedure given in (*d*) above.

(*h*) Operate the EQ2 FREQ Switch to the position that provides the best pattern.

(*i*) If the equipment is not ready to be turned over to operating personnel, operate the AC POWER switch (fig. 3-1) to off (down).

2-8.1. Equipment Alteration

NOTE

This special purpose alteration will be applied only to modems installed in oversea AUTODIN ASC's.

a. Disabling the TALK-REQUEST ALARM Circuit.

(1) Where the TALK-REQUEST ALARM function is not needed, it may be deactivated as follows:

(*a*) On PC board A6 locate R23.

(*b*) Unsolder and lift one end of R23, and insulate this free end.

(c) Short the TALK-REQUEST RESET switch 1A1S4 by soldering a short wire strap across its terminals.

(*d*) Place a note or tag on the modem to indicate that it has been altered to disable the TALK-REQUEST ALARM.

(2) This alteration must be retracted, and the altered circuits returned to their original condition before returning the modem to stock.

b. Strapping on the MX-73(*)/G.

(1) Strapping options for connector P1 (figs. 6-43, 6-44, and 6-45).

(*a*) Pins 13 and 14 (*n* and *w* on Assembly A8) are connected together when the MD-674(P)/G is connected to any equipment that sends a positive mark signal. This is the normal case and the MD-674(P)/G is strapped in this manner when received by the field.

(*b*) Pins 14 and 15 (*s* and *w* on Assembly A8) are connected together when the MD-674(P)/G is connected to any equipment that sends a negative mark signal.

(*c*) This strapping option is available only in the receive circuits of the MD-674(P)/G. For complete interface for equipment that utilizes a negative mark signal, a strapping option must also exist in the receive circuits of that equipment.

CHAPTER 3
OPERATION AND OPERATOR'S MAINTENANCE

3-1. Controls, Jacks, and Indicators
(fig. 3-1)

Control, jack, or indicator	Function
ALARM indicator	Lights to indicate signal failure.
DC POWER fuses:	
+15V 11/2A	Lights when blown; protects +15-volt dc power supply.
-15V 11/2A	Lights when blown; protects -15-volt dc power supply.
AC POWER:	
115/230V 3A fuse	Lights when blown; protects ac circuitry.
Indicator	Lights when ac power is applied.
ON switch	Two-position: ON-applies ac power to unit. OFF (down)-removes ac power from unit.
BAUD RATE switch	Four-position: selects baud rate **desired** for associated MX-73(*)/G.
TALK REQUEST RESET pushbutton.	Resets order-wire circuits for normal data operation.
TALK REQUEST:	
Pushbutton	Activates order-wire request signal.
Indicator	Lights when order-wire request signal is received.
LINE MONITOR jacks:	
RECEIVE	Allows external monitoring of received vf signal.
SEND	Allows external monitoring of send vf signal.
ORDER WIRE jacks:	
RECEIVE	Provides connection to teletypewriter receive equipment.
SEND	Provides connection from teletypewriter send equipment.

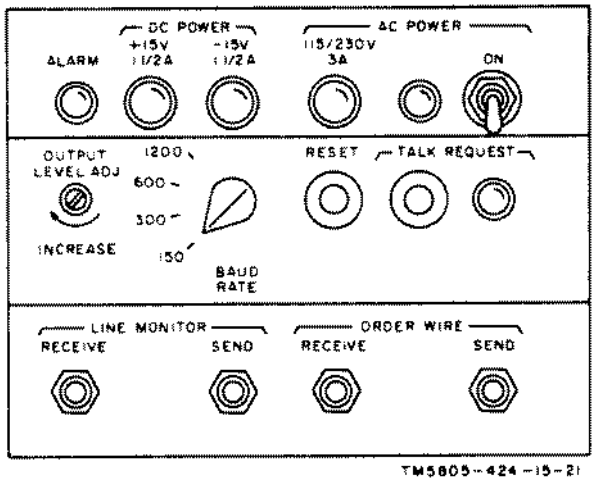


Figure 3-1. Front panel controls and indicators.

3-2. Starting and Stopping Procedures

Caution: **The OUTPUT LEVEL ADJ control and the BAUD RATE switch are preset during installation and initial adjustments. Do not change settings of either control in an operating system. Changing the setting of either control will interrupt system service.**

a. Starting.

(1) Set the BAUD RATE switch to the desired BAUD RATE position.

Note: The BAUD RATE switch may be set to the baud rate that corresponds with the baud rate of the MK-73(*)/G installed or any lower multiple of the MX73(*)/G baud rate.

(2) Operate the AC POWER switch to ON.

b. Stopping. Operate the AC POWER switch to the off (down) position.

3-3. Order-Wire Operation

a. Initiating Call.

(1) Plug the send cord of the teletypewriter into the ORDER WIRE SEND jack (fig. 3-1).

(2) Plug the receive cord of the teletypewriter into the ORDER WIRE RECEIVE jack.

(3) Momentarily depress the TALK REQUEST pushbutton.

(4) When the TALK REQUEST indicator lights, establish communications with the teletypewriter equipment.

(5) When communications are completed, momentarily depress the TALK REQUEST pushbutton.

(6) When the TALK REQUEST indicator lights, disconnect the teletypewriter equipment from the ORDER WIRE jacks, and momentarily depress the TALK REQUEST RESET pushbutton.

b. Receiving a Call.

(1) When the TALK REQUEST indicator lights, plug the send cord of the teletypewriter into the ORDER WIRE SEND jack, and the receive cord into the ORDER WIRE RECEIVE jack.

(2) Momentarily depress the TALK REQUEST pushbutton to send an acknowledgment signal to the distant operator.

(3) When the TALK REQUEST indicator lights to indicate that communications are completed, momentarily depress the TALK REQUEST pushbutton to send an acknowledgment signal to the distant operator.

(4) Disconnect the teletypewriter equipment from the ORDER WIRE jacks, and momentarily depress the TALK REQUEST RESET pushbutton.

3-4. Operation Under Unusual Conditions

Although the MD-674(P)/G retains its technical characteristics over a wide temperature and humidity range, adverse climatic conditions may affect operation. Observe the precautions given in *a*, *b*, and *c* below as appropriate.

a. Arctic Climates.

(1) Keep the equipment warm and dry.

(2) Keep the power on continuously, if possible.

(3) When equipment that has been exposed to the cold is brought into a warm room, moisture will gather on it; this may cause a change in operating characteristic When the equipment reaches room temperature, dry it thoroughly.

b. Tropical Climates. In tropical climates, the high relative humidity causes condensation on the equipment whenever the temperature of the equipment becomes lower than that of the surrounding air. To minimize this condition, provide as much ventilation as possible.

c. Desert Climate.

(1) The main problem in equipment operation in desert areas is the large amount of sand, dust, or dirt that enters the chassis of the MD-674(P)/G.

(2) Keep the equipment as free from dust as possible. Make frequent preventive maintenance checks (par 4-2). This equipment does not require lubrication and should be kept free from oil and grease.

3-5. Preventive Maintenance

To ensure that the modem is always ready for operation, inspect it systematically to discover and correct defects. The necessary preventive maintenance checks to be performed are listed in paragraph 3-6. Defects discovered during operation of the unit will be noted for future correction to be made as soon as operation has ceased. Stop operation immediately if deficiency is noted during operation which would damage the equipment. Records and reports of these checks and services must be made in accordance with the requirements set forth in DA Pam 738-750.

3-6. Operator's Preventive Maintenance Checks and Services Chart

NOTE

The checks in the "Interval" column are to be performed in the order listed.

B - Before operation

Item No.	*Interval B*	*Item to be inspected Procedure*	*Equipment is not ready/available if:*
1	*	Modem performance check. Perform operational checks as described in paragraphs 3-2 and 3-3.	Equipment fails to support assigned mission.

*Do this check before each deployment to a mission location. This will permit any existing problems to be corrected before the mission starts. The check does not need to be done again until redeployment.

CHAPTER 4
ORGANIZATIONAL MAINTENANCE

Section I. PREVENTIVE MAINTENANCE

4-1. Scope of Organizational Maintenance

a. General. Organizational maintenance is the systematic care, servicing, and inspection of equipment to prevent occurrence of trouble, reduce downtime, and maintain the equipment in serviceable condition. Preventive maintenance procedures are provided in paragraph 4-2. Troubleshooting procedures are provided in paragraphs 4-5 and 4-6 for isolation of system troubles, cable troubles, and troubles within the MD-674(P)/G. Defects that cannot be corrected must be reported to a higher category of maintenance personnel. Records and reports of repairs and preventive maintenance must be made in accordance with procedures given in DA Pam 738-750.

b. Preventive Maintenance Checks and Service Periods. Preventive maintenance checks and services are required monthly, under the following conditions:

(1) When the equipment is initially installed.

(2) When the equipment is reinstalled after removal for any reason.

c. Cleaning.

WARNING: **Adequate ventilation should be provided while using TRICHLOROTRIFLUOROETHANE. Prolonged breathing of vapor should be avoided. The solvent should not be used near heat or open flame; the products of decomposition are toxic and irritating. Since TRICHLOROTRIFLUOROETHANE dissolves natural oils, prolonged contact with skin should be avoided. When necessary, use gloves which the solvent cannot penetrate. If the solvent is taken internally, consult a physician immediately.**

(1) Use a dry, clean, lint-free cloth or brush to remove dust and dirt. If necessary, moisten the cloth, or brush with Cleaning Compound (Federal stock No. 6850-00-984-5853). After cleaning, wipe dry with a clean cloth.

WARNING: **Compressed air shall not be used for cleaning purposes except where reduced to less than 29 psi and then only with effective chip guarding and personnel protective equipment. Do not use compressed air to dry parts when TRICHLOROTRIFLUOROETHANE has been used. Compressed air is dangerous and can cause serious bodily harm if protective means or methods are not observed to prevent chip or particle (of whatever size) from being blown into the eyes or unbroken skin of the operator or of other personnel.**

(2) Dry, compressed air, not to exceed 60 pounds per square inch, may be used to remove dirt and dust from in accessible places.

d. Touchup Painting. Remove rust and corrosion from metal surfaces by lightly sanding them with fine sandpaper. Brush two thin coats of paint on the bare metal to protect it from further corrosion. Refer to the applicable cleaning and refinishing practices specified in TB SIG 364.

4-2. Preventive Maintenance Checks and Services

The preventive maintenance checks and services charts (para 4-3) outlines functions to be performed. These checks and services are to maintain Army electronic equipment in a combat serviceable condition; that is, in good general (physical) condition and in good operating condition. If a defect cannot be remedied by performing the corrective actions listed, higher category of maintenance or repair is required. Records and reports of these checks and services must be made in accordance with the requirements set forth in DA Pam 738-750.

4-3. Organizational Preventive Maintenance Checks and Services Chart

NOTE

The checks in the "interval" column are to be performed in the order listed.

M - Monthly

Item No.	*Interval M*	*Item to be inspected*	*Procedure*
1	*a*	Modem unit	Ensure that equipment functions properly as explained in chapter 3. If problems occur, perform troubleshooting and operational test procedures in chapters 5 and 6.
2	*a*	External cable assemblies	Ensure that cable assemblies are not loose or damaged.

a. As required

All data on page 4-3 deleted.

Section II. TROUBLESHOOTING AND REPAIR

4-5. Troubleshooting

a. General. The troubleshooting chart. given in *b* below is provided as an aid in localizing troubles in the MD-674(P)/G to parts (such as modules and printed circuit cards) authorized for organizational replacement. Only those corrective measures are given which organizational maintenance personnel can perform. If the measure suggested does not restore normal operation, troubleshooting at a higher category of maintenance is required. Note on the repair tag what corrective actions were taken and notify higher category maintenance personnel. All symptoms in the chart are obtained during normal operation, or during the operator's daily preventive maintenance checks and services and the organizational monthly preventive maintenance checks and services. If it is necessary to check voltages or waveforms at a specific pin of a printed-circuit card connector, remove the printed circuit card and insert the adapter card in its place. Plug the printed-circuit card into the adapter card and check the voltage or waveform.

b. Troubleshooting Chart.

Item No.	Trouble symptom	Probable trouble	Check and corrective measures
1	No indication on AC POWER indicator with AC POWER switch set to ON; blower motor does not operate.	*a.* Defective 115/230V 3A fuse (fig. 3-1). *b.* Defective power cable if necessary.	*a.* Replace fuse. *b.* Check power cable; and replace
2	No indication on AC POWER indicator with AC POWER switch set to ON; blower motor operates.	Defective AC POWER indicator	Replace indicator lamp.
3	AC POWER indicator lights with AC POWER switch set to ON, and blower motor does not operate.	Defective blower motor in power supply submodule (fig. 1-5).	Replace power supply submodule (pars 4-6).
4	All front panel indications normal, no indication at LINE MONITOR jacks, and order-wire inoperative.	*a.* Defective -15V 1-1/2A or +15V 1-1/2A fuse (fig. 3-1). *b.* Defective power supply ±15 volts printed-circuit card assembly A15. *c.* Defective power supply ±6 volts printed-circuit card assembly A14. *d.* Defective power supply sub-module (fig. 1-5).	*a.* Replace fuse. *b.* Check voltage at D.C. POWER +15V and -15V jacks (fig. 2-3); if incorrect, replace assembly A15 (fig. 1-6). *c.* Check voltage at D.C. POWER +6V and -6V jacks (fig. 2-3); if incorrect, replace assembly A14 (fig. 1-6). *d.* Replace power supply submodule.
5	No indication at LINE MONITOR SEND jack, no order-wire operation, and ALARM indicator lighted.	Defective transmit section	*a.* Check for input data at pins J and K of assembly A12 connector; if not present, replace assembly A12. *b.* Check for fsk ,signal at test jack J1 on assembly A18 through A32; if not present, replace MX-73(*)/G module (para 4-6). *c.* Check for fsk signal at test jack J2 on assembly A18 through A32; if not present, replace assembly A18 through A32 (MX-73(*)/G printed-circuit card).

Item No.	Trouble symptom	Probable trouble	Checks and corrective measures
			d. Check for fsk signal at pin V of assembly AT connector; if not present, replace assembly A7. *e.* Check for fsk signal at pin S of assembly A6 connector; if not present, replace MX-73(*)/G module (para 4-6). *f.* Check for fsk signal at pin V of assembly A6 connector; if not present, replace assembly A6. *g.* Check voltage at test jack J2 on assembly A3; if ground, replace assembly A3.
6	LINE MONITOR SEND jack indication normal, external no transition send alarm lighted, and common ALARM may or may not be lighted.	Defective assembly A12	Replace assembly A12.
7	LINE MONITOR SEND jack indication normal, and external loss-of-transmit-carrier alarm is lighted.	Defective assembly A6	Replace assembly A6.
8	Transmit bit-timing signals not available, but MD-674(P)/G operates normally in all other respects.	Defective assembly A5 .	Replace assembly A5.
9	No receive data supplied from MD-674(P)/G, but bit-timing signals are available.	Defective receive data section	*a.* Check for received fsk signal at test jack J2 on assembly A9; if not present, replace assembly A9. *b.* Check for fsk signal at jack J2 of assembly A25A3 connector (if used) and jack J1; if present at jack J1 and not J2, replace assembly A25A3; if not present at jack J1 or J2, replace assembly A9. *c.* Check for fsk signal at test jack J1 on assembly A8; if not present, replace MX-73(*)/G module (para 4-6). *d.* Check for fsk signal at pin M of assembly A8 connector; if not present, replace assembly A8. *e.* Check ;or digital data (sine wave) at pin L of assembly A8 connector; if not present, replace MX-73(*)/G module (para 4-6). *f.* Check for digital data at pin K of assembly A8 connector; if not present, replace assembly A8. *g.* Check for digital data at pin R of assembly A8 connector; if not present, replace MX-73(*)/G module (para 4-6). *h.* Check for digital data at pin Z of assembly A8 connector; if not present, replace assembly A8.

Item No.	Trouble symptom	Probable trouble	Checks and corrective measure
10	Receive data applied from MD-674(P)/G normally, but external no transition receive alarm is lighted.	Defective assembly A11	Replace assembly A11.
11	Receive data applied from MD-674(P)/G normally, but external receive carrier alarm is lighted.	Defective assembly A9	Replace assembly A9.
12	Receive bit-timing signals not available, but MD-674(P)/G operates normally in all other respects.	Defective assembly A5	Replace assembly A5.
13	Receive data cannot be regenerated, but bit-timing signals are normal.	Defective assembly A11	Replace assembly A11.
14	No receive data applied from MD-674(P)/G, receive bit-timing signals not available, but transmit bit-timing signals are available.	Defective assembly A3 or A4	Check for square-wave output at test jack J1 on assembly A4; if not present, replace assembly A3; if present, replace assembly A4.
15	No receive data applied from MD-674(P) /G and no bit-timing signals available.	Defective OA-8072/G module or printed-circuit card, or assembly A1 or A2.	If internal crystal oscillator is used, check for timing signals at test jacks J1 and J2 on assembly A33A2. If .not present at J1, replace assembly A33A1 (para 4-6). If present at J1 but not at J2, replace assembly A33A2. Check for timing signals at test jacks J1 and J2 on assembly A2; if not present at J1, replace assembly A1; if present at J1, but not at J2, replace assembly A2.
16	Order-wire circuit operation cannot be initiated; all other modes of operation are normal.	Defective assembly A3	Replace assembly A3.
17	Order-wire circuit operation cannot be detected; all other modes of operation are normal.	Defective assembly A10	Replace assembly A10.
18	TALK REQUEST indicator does not light during normal order-wire circuit operation.	Defective indicator lamp	Check and replace lamp.
19	Common ALARM indicator lamp does not light during normal alarm condition.	*a.* Defective indicator lamp *b.* Defective assembly A12	*a.* Check and replace lamp. *b.* Replace assembly A12.

4-6. Replacement of Parts

a. Modules.

Caution: **When removing or replacing the power supply module, be careful not to damage the rfi honeycomb air filter mounted on the rear of the front panel.**

(1) The power supply submodule (fig. 1-5) and the MX-73(*)/G module (fig. 1-6) are plug-in modules that are secured with quick-release fasteners. To remove either module, loosen the quick-release fasteners and pull the module straight out from the chassis. To replace either module, properly align the module, insert it into the fasteners.

(2) The OA-8072/G module (fig. 14) is secured with hexagonal nuts. To remove the module, remove the hexagonal nuts

and pull the module straight out from the chassis. To replace, insert it into the chassis, and secure it to the chassis with the hexagonal nuts.

b. Air Filter.

(1) Remove the power supply submodule (*a* (1) above).

(2) Remove the screws, washers, and nuts that secure the air filter to the rear of the front panel and remove the air filter.

Caution: **Be careful not to damage the rfi gasket cemented to the air filter if the air filter is to be cleaned and replaced.**

(3) Clean the air filter (para 4-1*c*) or obtain a replacement air filter and reposition the air filter on the rear of the front panel.

(4) Secure the air filter with the screws, washers, and nuts. Be sure the screws are securely tightened.

(5) Replace the power supply submodule (*a* (1) above).

c. Rf Gaskets. Rfi gaskets must be replaced as a single piece. Before replacing an rfi gasket, be sure the surface is thoroughly cleaned to insure electrical continuity. Tighten all screws securely to insure good electrical continuity.

CHAPTER 5
FUNCTIONING OF EQUIPMENT

Section I. BLOCK DIAGRAM ANALYSIS

5-1. General

The purpose, operation, and interoperation of the various circuits in this equipment are explained in paragraphs 5-2 through 5-24. Familiarity with the equipment, how it works, and why it works that way are valuable tools for troubleshooting the equipment rapidly and effectively. Circuits of the MD-674(P)/G fall into three basic groups: send, receive, and timing. The send circuits convert binary input data, or telegraph (order-wire operation), into a fsk signal suitable for transmission; mark and space frequencies are determined by the type of MX-73(*)/G used. The receive circuits convert fsk input data to either binary or teletypewriter data, and also provide for regeneration and retiming of the received input signals. The timing circuits supply timing signals necessary for the MD-674(P)/G and for external transmitting and receiving equipment.

5-2. Send Circuits

(fig. 8-4)

a. Send Data. When set to DATA, the INPUT SELECT switch passes the send data signal or order-wire signal from the ORDER WIRE SEND jack to the input interface amplifier, which shapes the input data signal and applies it to the tone oscillator control. Depending on the, sense of the input data, the tone oscillator control enables either the mark oscillator or the space oscillator. The mark and space output frequencies are divided by an appropriate binary divider to the correct channel mark and space frequencies. The two frequencies (fsk signal) are then applied through the transmit filter. which removes any undesired frequencies, to the output amplifier. The output amplifier provides for an output level adjustment of the output fsk signals, which are then supplied to the external transmitting equipment.

b. Send Alarms.

(1) If the input send data to the MD-674(P)/G is lost, the input interface amplifier provides a steady voltage to the no-transition alarm sensor, which consequently applies a voltage to the 5-second delay, actuating the delay circuits. If no data transitions occur within 5 seconds (or longer), the common alarm circuitry provides a ground to light the ALARM indicator lamp. The 5-second delay contains a control (TRANSITION ALARM TIME TRANSMIT) for fine adjustment of the delay circuits. When the input data transitions are restored, removal of the voltage applied to the 5-second delay removes the ground from the ALARM lamp which extinguishes the lamp.

(2) If the send carrier signal is not applied to the output amplifier (fsk mark and space frequencies), the failure is detected by the loss-of-carrier alarm sensor, which then provides an activating voltage to the 2-second delay. If the carrier signal is lost for at least 2 seconds, the 2-second delay output causes the common alarm circuitry to light the ALARM indicator lamp. The XMIT CARRIER ALARM THRESHOLD control sets the minimum amplitude requirements of the carrier signal; any signal below this set level causes an alarm 2 seconds after the condition persists. When the level is restored to normal, the activating voltage is removed from the 2second delay, which removes ground from the ALARM lamp, extinguishing the lamp.

5-3. Receive Circuits

(fig. 8-4)

a. Receive Data. Of the receive fsk data applied through the input amplifier, only the proper channel

frequencies are passed by the receive filter to the second input amplifier, which shapes the input signals. The demodulator circuit converts the fsk signals to binary data marks and spaces, at a constant signal level. that are applied to the timing bistable. The timing bistable, in conjunction with the timing circuits (para 5-4 below), supplies a retimed and reshaped (regenerated) data signal to the output driver for application to the external receiving equipment.

b. Receive Alarms.

(1) If the input fsk signals are lost, or fall below a predetermined level as determined by the REC CARRIER ALARM THRESHOLD controls, the second input amplifier applies an alarm-voltage level to the loss-of-carrier-alarm sensor, activating the 2-second delay. If the alarm condition persists for at least 2 seconds, the 2-second delay output causes the common alarm circuitry to provide a ground that lights the ALARM indicator lamp. Restoration of the input data removes the activating signal from the 2-second delay, which removes the ground from the ALARM lamp, extinguishing the lamp.

(2) If the recovered data signal is lost in the receive circuits and no transitions are applied to the output driver, the timing bistable remains in a reset condition due to timing circuit inputs, applying a constant voltage level to the no-transition alarm sensor. This sensor interprets the constant voltage level as an alarm condition and applies an activating vto the 5-second delay output activates the common alarm circuitry, thereby providing a ground to cause the ALARM lamp to he lighted. The 5-second delay contains a control (TRANSITION ALARM TIME RECEIVE) for fine adjustment of the delay circuits. When the data transitions are restored, the activating voltage is removed from the 5-second delay, extinguishing the ALARM lamp.

5-4 Timing Circuits

(fig. 8-4)

These circuits supply bit-timing signals for the external transmitting and receiving equipment and for the timing bistable in the MD-674(P)/G receive circuits, to provide an undistorted, phased-corrected output data signal. Internal timing signals may be supplied by an internal 1.2288-mega-cycle (mc) clock oscillator or by an externally applied bit-timing input signal.

a. The internal clock oscillator output frequency is divided by 8, in a three-stage binary divider, and is applied to the clock option straps. If externally applied, the bit-timing signal activates the variable-control oscillator and thus provides timing signals to the clock option straps.

b. Whichever timing is used, a 153.6-kc signal is applied through the clock option straps to another three-stage binary divider which, in conjunction with the BAUD RATE switch, provides a timing signal frequency at 128 times the desired bit-rate. The selected 128 times bit-timing signal is applied from the BAUD RATE switch to the divide-by-128 countdown chain and to add-subtract correction logic.

(1) A 7-stage binary counter, the divide-by128 countdown chain, divides the input frequency by 128. Countdown chain output provides bit-.timing to the output drivers, which supply an uncorrected bit-timing signal to the external data transmitting equipment.

(2) Add-subtract correction logic recovers received timing from the received input signal, comparing the resulting generated timing signal transitions with the received data transitions from the demodulator circuits; therefore, this logic controls the counting operation of the second divide-by-128 countdown chain; it adds timing pulses to the chain if the generated timing signal is too slow, and it subtracts timing pulses if the generated timing signal is too fast. By this corrective action, the bit-timing signal output of the divide-by-128 countdown chain is kept in phase (synchronized with the received data. The corrected bit-timing signal may be used by the timing bistable to regenerate and retime

the data output signal (strap option); it is also applied to external receiving equipment that require a phase-corrected, bit-timing signal.

5-5. Order-Wire Circuits
(fig. 8-4)

a. When the TALK REQUEST pushbutton is depressed, the talk-request send circuits apply a 1.5-second inhibit voltage to the send circuit binary divider. With the binary divider inhibited for 1.5 second, the data output terminals remain in a steady mark condition, which will be interpreted at the other station as a talk-request signal (*b* below). The 1.5-second inhibit voltage also inhibits the loss-of-carrier alarm, preventing an alarm indication as a result of loss-of-the-carrier signal (such loss being caused by the inhibit placed on the binary divider).

b. When a talk-request signal (1.5-second loss of carrier) is received by the low speed modem receive circuits, the loss-of-carrier-alarm sensor activates the talk-request receive circuits. The latter therefore provides an inhibit voltage to the loss-of-carrier-alarm sensor, preventing an alarm indication (due to loss-of-carrier). Output of the talk-request receive circuits is also applied to the retiming option select circuits, where the retiming of the received data may be switched in or out automatically if desired (strap option). The talk-request receive circuit also applies a ground to light the TALK REQUEST indicator lamp. Teletypewriter transmitting equipment is jacked-in through the ORDER WIRE SEND jack and receiving equipment is jacked-in to the ORDER WIRE RECEIVE jack. Operation with teletypewriter data is the same as that for normal data, as described in paragraphs 5-2 and 5-3.

Section II. CIRCUIT ANALYSIS

5-6. General

a. Because many MD-674(P)/G stages are similar, and in some cases identical (except for reference designations and component values), a circuit analysis of each individual stage is not provided in this technical manual. Instead, a circuit analysis of digital circuit types (with associated logic symbol and pertinent waveforms) is presented in this section, a circuit analysis of all analog circuitry used in the equipment is presented in section III, and a complete logic-block diagram analysis is provided in section IV.

b. Reference designations such as C_a, R_c, and Q_a, used with the circuit descriptions in this section (figs. 5-1 through 5-7), are arbitrarily assigned for the circuit analysis. To determine the correct reference designations for a part associated with a particular stage, refer to the applicable schematic diagram (figs. 8-6 through 8-27). Reference designations such as FF-, GAI-, and GOI- (figs. 5-1 through 5-7) are arbitrarily assigned to the logic symbols for the logic analysis (section IV).

c. For detailed analysis of logic circuits described in section IV, refer to TM 11490.

5-7. Bistable Multivibrator Stages

a. General. The function of each bistable multivibrator stage is basically the same and the logic symbol shown directly under each and used with the logic diagram (fig. 8-5) is basically the same. The reference designations for the logic symbols differ to indicate how the bistable is triggered. The lines on the left side of the logic symbol represent the inputs; the lines on the right side represent the outputs. The upper lines (left and right) of the logic symbol are associated with one transistor in the stage, and the lower lines are associated with the other transistor of the stage.

b. Common Input Bistable Type FFA- (A, fig. 5-1).

(1) *General.* Resistors R_e and R_f establish initial bias for transistors Q_a and Q_b, respectively. Resistors R_c and R_d provide the necessary cross-coupling to allow the stage to change state. The output (180° out of phase with each other) are developed across the collector and emitter of the transistors, with resistors R_a, and R_b acting as collector load resistors. Diodes CR_a and CR_b clamp the output voltage to -6 volts when either transistor is cut off.

(2) Triggering. To be triggered, the stage shown in A, figure 5-1, requires positive input pulses. Resistor R_g, capacitor C_a, and diode CR_c form a differentiating AND gate. With a positive level applied

to the input of R_g and C_a, a differentiated waveform (positive and negative spikes) is applied to diode CR_c, which passes only the positive spike to the base of transistor Q_a. Resistor R_h, capacitor C_b, and diode CR_d perform the same function for transistor Q_b. If the transistor associated with the positive inputs is conducting when the positive trigger is applied through its associated base diode, the transistor will be cut off, causing the other transistor to conduct, and thus change the state of the bistable. A second positive trigger must now be applied to this on transistor to change the state of the bistable (that is, set it to its original state).

c. Common Input Bistable With Collector Steering, Type FFC- (B, fig. 5-1). The bistable multivibrator stage shown in B, figure 5-1, is essentially the same as that shown in A, figure 5-1, except that collector steering resistors R_g and R_b are used to direct the common positive input to the transistor that is conducting.

d. Two-Input Bistable-Type FFE- (A, fig. 5 2).

(1) *General.* Resistors R_a. and R_b establish initial bias for transistors Q_a, and Q_b, respectively. Resistors R_d and R_e provides the necessary cross-coupling to allow the stage to change state. The outputs (180°out of phase with each other) are developed across the collector and emitter of transistors Q_a and Q_b, with resistors R_f and R_g, acting as the collector load resistors. Capacitor C_a is used as a speedup capacitor to insure rapid changeover when transistor Q_a is triggered.

(2) *Triggering.* Resistor R_c serves as a limiting resistor for one of the positive trigger inputs, with diode CR, used to pass only the positive input transitions. The input to the base of transistor Q_a is a positive trigger developed by the previous stage.

e. Two-[n7pt Bistable with +6 Volt Output clamp, Type FFF- (B, fig. 5-2).

(1) General. Operation of the FFF-type bistable is essentially the same as that of the FFE-type bistable (*d* above). For the FFF-type, however, the output voltage is clamped to -6 volts instead of ground when the transistors are conducting, and positive triggering is achieved in a different way ((2) below).

(2) Triggering. Diode CR_a and resistor R_b and diode CR_b and resistor RC limit the input trigger to a +6-volt positive trigger. Resistor R, develops one input trigger, while capacitor C_a provides a differentiated input to diode CR_b.

f. Two-Input Bistable With Internal Gating and -6-Volt Output Clamp, Type FFD- (A, fig. 5-3).

(1) *General.* Resistors R_c and R_d establish the initial bias for transistors Q_a and Q_b, respectively. Resistors R_a and R_b are the collector load resistors. Resistors R_e and R_f and capacitors C_a and C_b provide for cross-coupling and determine the switching time for the stage to change state. The outputs (180°out of phase with each other) are developed across the collector and emitter of the two transistors. Diodes CR_a and CR_b clamp the output to -6 volts when the transistors are cut off.

(2) *Triggering.* Resistor R_g, capacitor C_c, and diode CR_c form a shaping AND gate that provides positive triggers, exclusively, to the base of transistor Q_a only when Q_a is conducting (the positive trigger will turn Q_a off). Resistor R_h, capacitor C_d, and diode CR_d, perform the same function for transistor Q_b when Q_b is conducting.

g. Two-input Bistable With Internal Gating, -6-Volt Output Clamp, and Collector Steering, Type FFG- (B, fig. 5-3). The FFG-type of bistable is essentially the same as the FFA-type (*b* above), except that, for the FFG-type, either one of two inputs may be applied as a common input to both transistors Q_a and Q_b. Diodes CR_e and CR_d provide for collector steering of both common inputs, allowing a positive trigger to be applied through diode CR_c or CR_d (one input) or through diodes CR_f or CR_g (second input), the path depending on which transistor is conducting. Each output is clamped to -6 volts (by diode CR_a or CR_b) when a transistor is cut off.

h. Two-input Bistable With +6-Volt Output Clamp, Type FFB- (fig. 5-4). The stage shown in figure 5-4 is essentially the same as the FFE

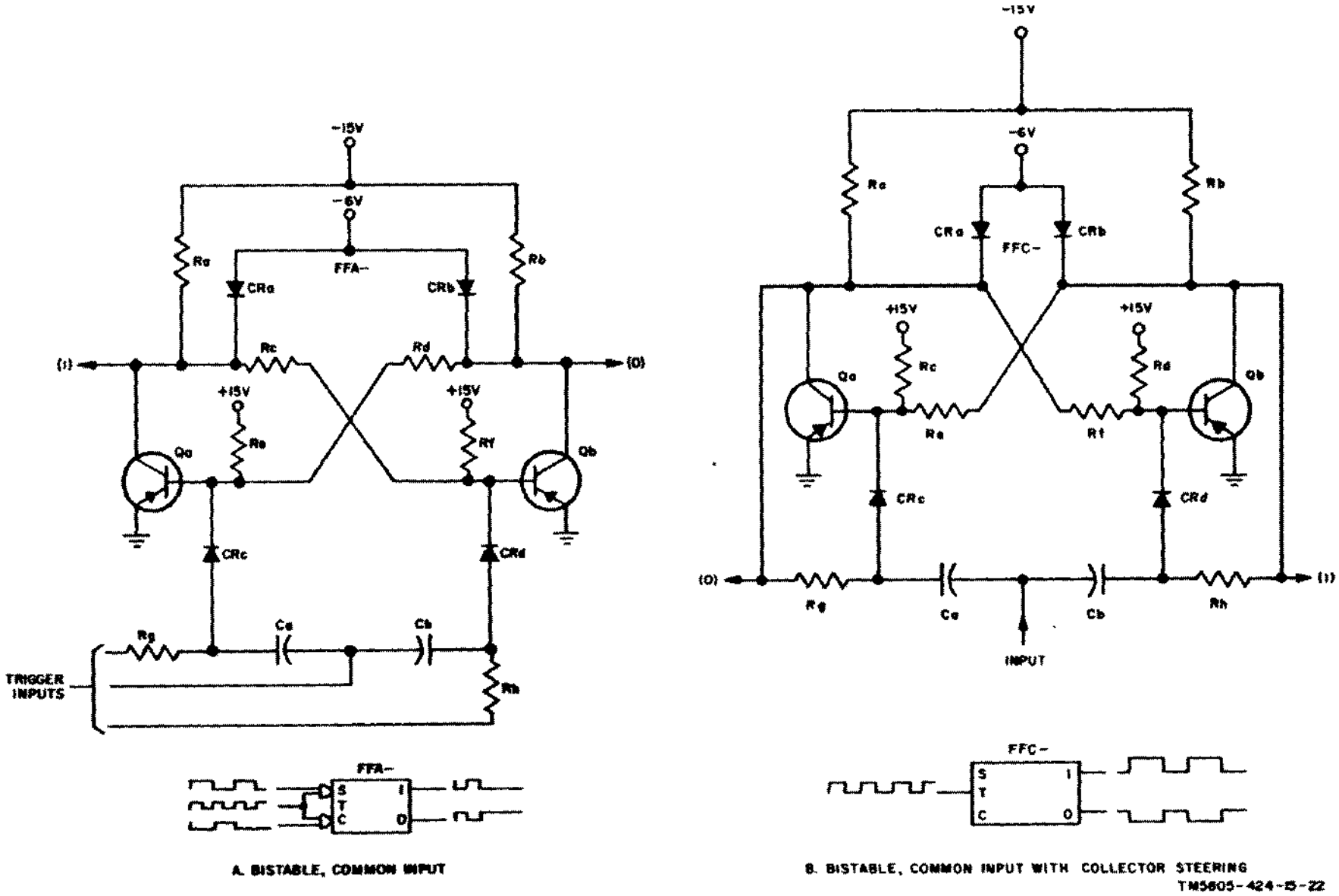


Figure 5-1. Common input bistable stages, schematic diagram and logic symbol.

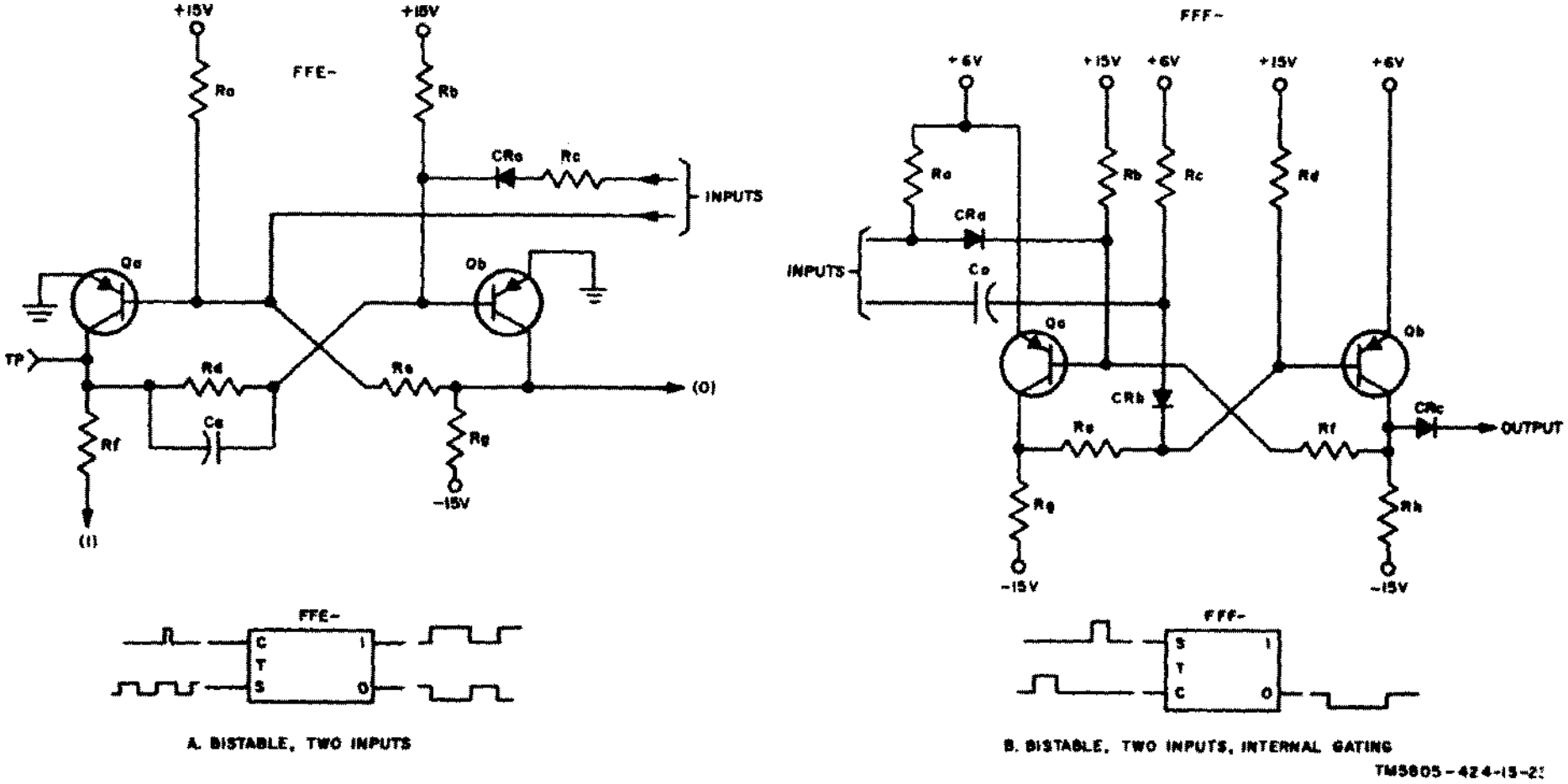


Figure 5-2. Two-input bistable stages schematic diagram and logic

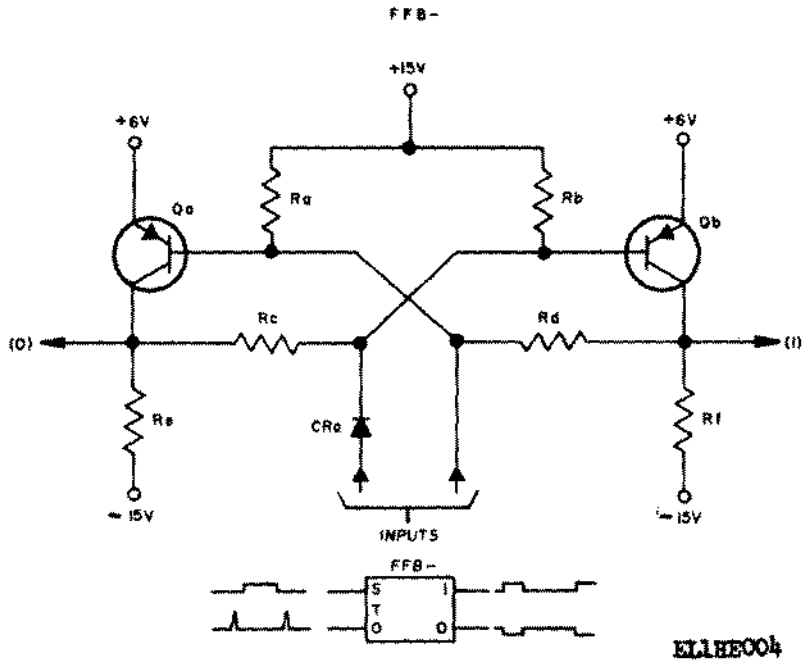


Figure 5-4. Two-input bistable stage, +6-volt clamped output, schematic diagram and logic symbol

type (*d* above), except that when the FFB-type transistors conduct, the output is held at +6 volts instead of ground, and no limiting resistor is used in the input circuit of transistor Q_b.

5-8. AND Gate Stages
(fig. 55)

a. General. Four basic variations of AND gate stages are used in the equipment. Two are inverting gates and two are noninverting gates. Since the function of the stages is essentially the same, the same basic logic symbol is assigned every stage. Differences in the logic symbols denote whether the required inputs to activate the stage are low level (circle at the inputs of the logic symbol) or high level (no circle at the inputs), and whether the activated (enabled) output is low level (circle at the output of the logic symbol) or high level (no circle at the output).

b. Circuit Analysis. An AND gate will develop a proper output when coincident input pulses of the same polarity are present on the input lines.

(1) The GAD-type AND gate (A, fig. 5-5) requires the two low-level inputs which are blocked by diodes CR_a and CR_b, in order to provide a low-level output (no current flows through resistor R_b). Resistor R_a serves as a limiting resistor. If either input is a high level (ground), the applicable diode conducts, providing a high level (ground) at the output, with resistor R_b dropping the 15 volts from the supply.

(2) In the GAS-type AND gate (B, fig. 5-5), capacitor C_a differentiates its input square wave, and diode CR_a passes only the positive spike if the input to resistor R_a is also a high level. If the input to resistor R_a is a low level, capacitor C_a can never charge above ground and no output is available.

(3) Two GAI-types of AND gate are used in the equipment.

(*a*) The type shown in C, figure 5-5, requires two high-level inputs (ground) to hold transistor Q_a cut off, providing a low-level (-15 volts) output. A low level applied to either input is passed by its appropriate diode (CR_a or CR_b) to the base of transistor Q_a, turning Q_a on and providing a high-level (ground) output. Resistors R_a and R_b provide initial bias for the transistors. Resistor R_c

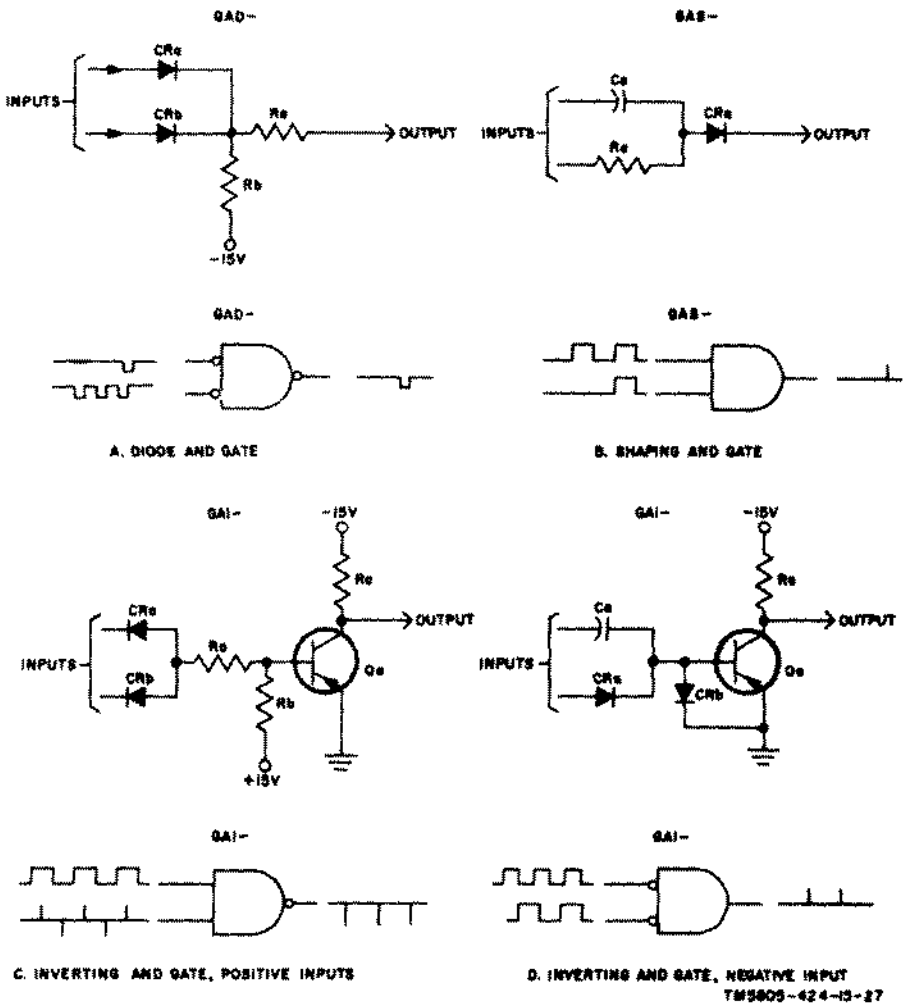


Figure 5-5. AND gate stages, schematic diagram and logic symbol.

acts as the collector load resistor for transistor Q_a.

(*b*) The GAI-type AND gate shown in D, figure 5-5, requires two low-level (-15 volts) inputs to provide a high-level output. A low-level applied to diode CR_a is blocked (acting as an open circuit), so input capacitor C_a controls circuit operation, turning transistor Q_a on when the input is negative (providing a high-level [ground] output), and turning it off when the input is positive (providing a low-level [-15 volts] output). If the input to diode CR_a is a high level, the high level is passed by the diode to the base of transistor Q_a, maintaining it at cut off, regardless of the condition of the input signal applied to capacitor C_a. Diode CR_b limits the forward bias of transistor Q_a, and resistor R_a is the collector load resistor.

5-9. OR Gate Stages
(fig. 5-6)

a. General. Several types of OR gate stages are used in the equipment, all identical in operation. The only difference is in the input and output circuit configuration. In all cases, a high-level input on any

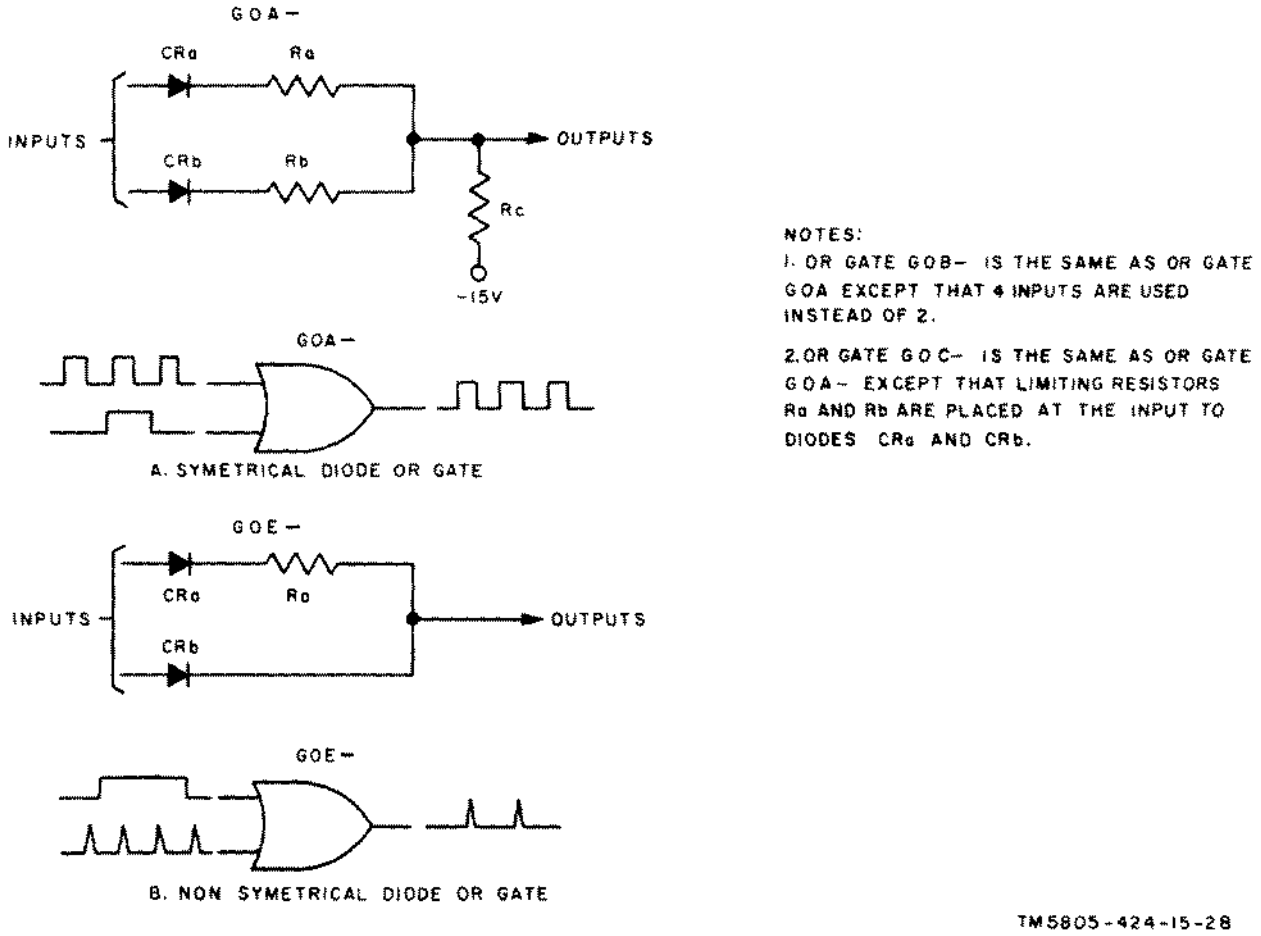


Figure 5-6. OR gate stages, schematic diagram and logic symbol.

put on any input line provides a high level at the output.

b. Circuit Analysis. The input diodes pass only the high-level signals, and the input resistors act as series limiters to protect subsequent circuitry. The enabled output of each gate is a high level (ground). The inhibited output of OR gates GOA-, GOB-, and GOC- is a low-level -15 volts; the inhibited output of OR gate GOE is absence of output (open circuit).

5-10. Amplifier Stages
(fig. 5-7)

a. General. Two types of digital amplifier circuits are used in the equipment: the inverting type IN-, which provides output inversion of the input signal, and the noninverting or emitter follower type AM-.

b. Circuit Analysis.

(1) In the amplifier circuit shown in A, figure 5-7, resistor R_a is a limiting resistor and may be bridged by speedup capacitor C_a. Resistor R_c provides initial bias for the stage, and resistor R_b is the collector load resistor. Optional diode CR_b acts to limit the forward bias of transistor Q_a. Optional diode CR_b acts to clamp the cutoff output to -6 volts.

(2) In the amplifier circuits shown in B, figure 5-7, PNP transistor Q_a (left side) uses resistor R_a as the emitter-load resistor to provide a low-level output. NFN transistor Q_a (right side) is used to provide a low-level output (developed across emitter resistor R_c). An NPN transistor is used in some cases to provide a high

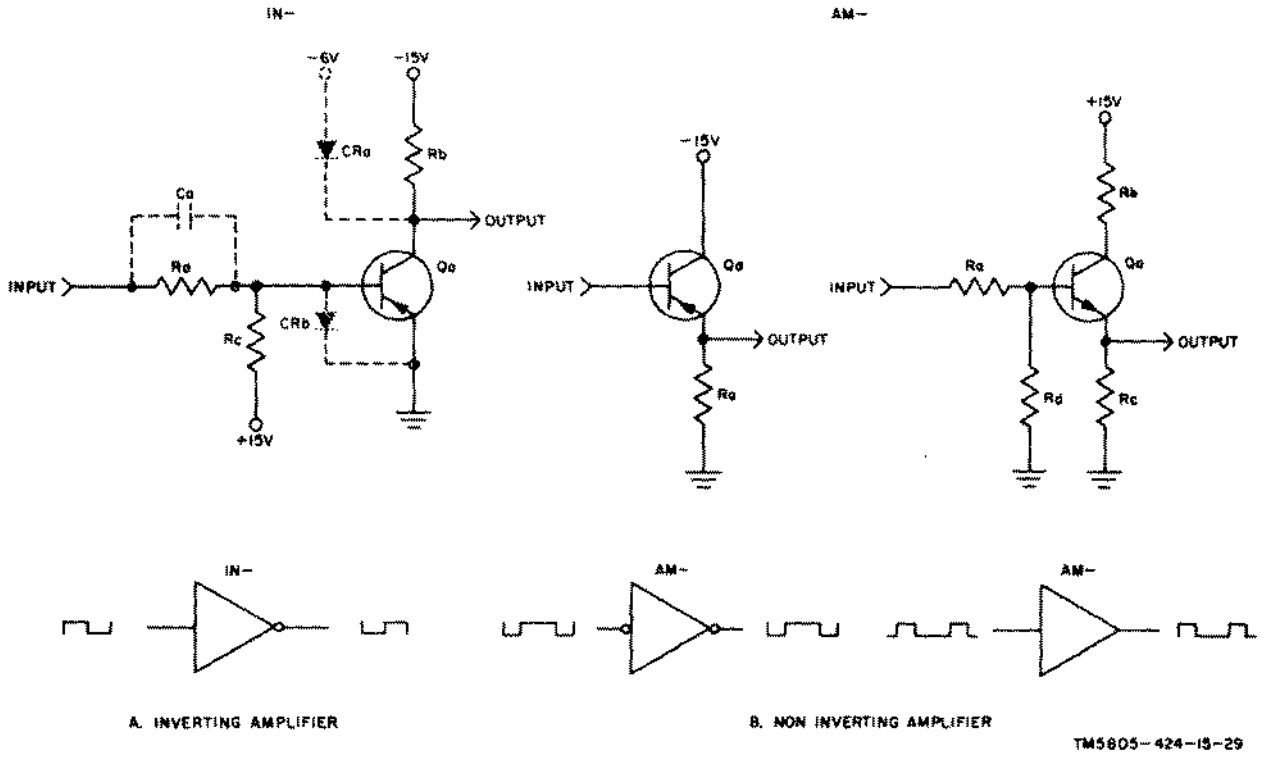


Figure 5-7. Amplifier stages, schematic diagram and logic symbol.

level output (developed across emitter resistor R_c). Resistors R_a and R_d may be used to establish initial operating bias for the stage; resistors R_b and R_c act to limit the output voltage when transistor Q_a conducts.

Section III. ANALOG CIRCUIT ANALYSIS

5-11. Oscillator Circuits
(fig. 8-21)

a. The oscillator circuits used to develop mark and space frequencies for the transmitted frequency-shift-keying (fsk) data are identical Colpitts-type, crystal-controlled oscillators, except for the crystal type and values of frequency-determining components (capacitors C1 through C4 and inductor L1 and capacitors C6 through C9 and inductor L2). These component values are chosen according to the required output frequencies. Only oscillator circuit Y1 (OSC-1) is discussed in *b* below.

b. Crystal Y1, capacitors C1 through C4, and inductor L1 are the frequency-determining components. Capacitor C5 provides the necessary feedback to amplifier transistor Q1, to sustain oscillations. Resistor R1 is the collector load resistor, R2 furnishes initial bias for the oscillator stage, and R3 is the direct-current (dc) coupling resistor to emitter follower Q2. Resistor R4 is the emitter self-biasing resistor for transistor Q2, used as a buffer between the oscillator circuit and the output load to prevent the undesired effects of loading.

5-12. Oven Regulator
(fig. 8-21)

a. The oven regulator circuits maintain the oscillator oven temperature at a constant level to provide maximum stability for the oscillator circuit. OVEN TEMP ADJUST resistor 1A1R1, in conjunction with resistor 1A1R2, sets the initial bias for transistor Q1. The resistance of thermistor A1RT1 varies inversely with the external temperature; it provides greater current through transistor Q1 when external temperature decreases

and less current when the external temperature increases. Transistors Q1 and Q2 form a differential amplifier that provides a constant emitter voltage. The constant emitter voltage serves as the forward bias for transistor Q1, thereby allowing the maximum current variations required by thermistor 1A1RT1. Resistor R1 is the collector resistor for transistor Q1. When transistor Q1 current increases, its collector voltage becomes more negative and increases the forward bias on transistor A1Ql and therefore the current flow through the heater element. Diode CR1 functions as the emitter resistance for transistor 1A1Q1. Resistors 1A1R3 and 1A1R5 form a voltage divider to establish initial bias for transistor Q2.

b. If thermistor 1A1RT1 senses a rise in the external temperature, its resistance decreases, so that less current flows through transistor Q1. Consequently, the potential at the collector of transistor Q1 becomes more positive, which increases the reverse bias on transistor 1A1Q1and decreases the current flow through the heater element.

5-13. Transmit Output and Carrier Alarm Circuits
(fig. 8-11)

a. Data Circuit. Input, fsk signals are applied through OUTPUT LEVEL ADJ resistor 1A1R6 to the output amplifier stage. Transistors Q1 and Q2 form a differential amplifier. Base resistor R2 develops the input signal, emitter resistor R3 develops initial bias for the differential amplifier, and resistors R4 and R6 are the collector load resistors for transistors Q1 and Q3. Coupling transformer 1A1T2 is a 1-to-1 current ratio transformer, and capacitor C1 and resistor R5 form a low-frequency alternating-current (ac) sensing network that provides degenerative feedback to transistor Q2. The degenerative feedback on transistor Q2 forces transistor Q3 to assume the same high impedance for both the mark and space frequencies, thus making the output at the secondary of transformer 1A1T2 proportional to the input voltage (signal) to transistor Q1, regardless of the input signal frequency. Resistor R7 is the collector load for transistor Q3. The output signal from transformer A1T2 is applied to BALANCED XMTR CARRIER OUTPUT terminals 12 and 13 of terminal board TB2. Diodes CR12 and CR13 permit output transformer 1A1T1 to operate with a high-impedance output line. OUTPUT switch 1A1S7 (in the 600~position) connects resistor R38 across diodes CR12 and CR13 to allow operation into a 600-ohm output line.

b. Alarm, Circuit. The alarm circuit consists of the level threshold circuit, the amplitude detector circuit, the 2-second delay circuit, and amplifier IN-8.

(1) *Level threshold circuit.* In this degenerative amplifier (transistors Q4 and Q5), capacitor C2 and resistor R10 suppress any oscillations that may occur. A positive-going signal applied to the base of transistor Q4 increases Q4 conduction, reducing its collector voltage. This action reduces the forward bias on transistor Q5; thereby decreasing Q5 conduction. Resistors R12 and R15 are emitter swamping resistors; resistors R9, R13, and R14 form the collector load for transistor Q5. THRESHOLD resistor 1A1R14 sets the minimum level requirements of the circuit that will provide sufficient output signal amplitude to operate the amplitude detector circuit ((2) below).

(2) *Amplitude detector circuit.* This is basically a paraphrase amplifier (transistor Q6) and a bridge rectifier circuit, followed by a regenerative amplifier (transistors Q7 and Q8). Resistors R16 and R17 provide initial bias and develop the input signal; capacitor C3 is the coupling capacitor. Transistor Q6 provides two outputs, 180° out of phase with one another, that are coupled through capacitors C4 and C5 to the bridge rectifier (CR1 through CR4). Diodes CR5 and CR6, together with resistor R21, provide for a slight forward bias to diodes CR2 and CR3. Resistors R18 and R19 are the load resistors for the paraphrase amplifier. As long as an input signal of sufficient amplitude is applied to transistor Q6, a slight positive voltage will be applied to the base of transistor Q7 through either diode CR1 or CR4, depending on the polarity of the input signal. When the input signal is removed, transistor Q6 is cut off and the bridge rectifier produces no output; the

voltage applied to the base of transistor Q7 is now highly negative, limited by the current flow through resistor R22 and the charge on capacitor C6 (approximately -9 volts). The negative voltage turns Q7 on and provides a positive level to the base of transistor Q8; thereby cutting off transistor Q8. Resistor R24 is the common emitter load resistor, resistors R26 and R28 are the collector load resistors for transistors Q7 and Q8, respectively, and resistors R27 and R25 provide for initial forward bias for transistor Q8 when data input signals are applied to the amplitude detector.

(3) *2-Secoond delay circuit.*

(*a*) With data signals applied to the amplitude detector, transistor Q7 is cut off and Q8 is conducting ((2) above), causing transistor Q9 to conduct. Resistor R29 drops sufficient voltage to provide a forward bias for transistor Q9. With transistor Q9 conducting, capacitor C7 does not charge; consequently, a ground is applied to the Q10 base, which cuts off transistor Q10. With transistor Q10 cut off, +15 volts is applied to the base of transistor Q11, which cuts off transistor Q11 and supplies -6 volts to the alarm circuits (no alarm).

(*b*) When input data is removed from the amplitude detector, transistor Q7 conducts and transistor Q8 cuts off ((2) above) ; this action causes transistor Q9 to cut off and allow capacitor C7 to charge toward +15 volts. When the charge on capacitor C7 reaches a sufficient potential, diode CR9 becomes forward biased, causing transistor Q10 to conduct, grounding the base of transistor Q11, and thus causing Q11 to conduct.

(*c*) With transistor Q11 conducting, +6 volts is applied to the alarm circuits, which activates the alarm. When the input signal to the amplitude detector is restored, capacitor C7 discharges, cutting off transistor Q10 and thus 5-12 applying -6 volts to the alarm circuits ((*a*) above).

(4) *Amplifier INV- circuit.* Amplifier IN-8 inverts the output of transistor Q11, providing +6 volts to the output during the no-alarm condition, and providing ground during the alarm condition. Diode CR10 clamps the output voltage from transistor Q12 to +6 volts when transistor Q12 is cut off. Resistor R36 is the base current-limiting resistor, and resistor R37 is the collector load resistor.

5-14. Receive Input and Carrier Alarm Circuits

(fig. 8-14)

a. General. The receiver input circuits consist of two input amplifiers, used in conjunction with receive filter FIL1, and an optional delay equalizer module (para 5-18). The alarm circuits consist of a level threshold circuit, an amplitude detector circuit, three amplifiers, an OR gate, and a 2-second delay circuit.

b. Receive Input Circuit. Input fsk signals are applied through transformer 1A1T3 to amplifier transistor Q1. Transistor Q1 is basically an emitter follower, with capacitor C1 as the collector bypass. Resistor R5 is the collector current limiting resistor, and resistor R1 is the emitter load resistor. The amplifier input signal is applied through dc coupling resistor R3 to a load resistor in receive filter FL1, and directly to the delay equalizer circuit, if used (par 5-18). The signal is fed from FL1 (pin 26) or the delay equalizer circuit to second input amplifier Q2, Q16, a degenerative amplifier that impedance matches receive filter FL1. Resistors R2 and R4 provide linear biasing of the stage, resistors R47 and R49 are the collector load resistors, and resistor R48 is the emitter load resistor. The second input amplifier output is applied to receive filter FL1, which passes only the desired channel frequencies to the demodulator circuits (para 5-16).

c. Alarm Circuits.

(1) The demodulator signal is applied to third input amplifier Q15 (an emitter follower that provides a low impedance to level threshold coupling capacitor C2) and applied to REC CARRIER

ALARM THRESHOLD control resistor 1A1R11. Resistor R50 is the emitter load resistor for transistor Q15.

(2) The level threshold is a degenerative operational amplifier (Q3, Q4, and Q5) with an emitter follower (Q6) output. The signals that are applied to transistor Q3 are amplified, inverted, and fed to transistor Q5. Transistor Q4 provides degenerative feedback for transistor Q6. Resistor R11 and capacitor C3 form a shelf network that allows transistor Q5 sufficient time to change amplification levels without developing unnecessary phase shifting between the input and output signals. Resistor R13 is the common emitter resistor for transistors Q3 and Q4, resistors R9 and R10 set the operating bias for transistor Q5, and resistor R12 is the collector load resistor for transistor Q5. Resistors R14 and R16 form a voltage divider network that limits the amount of degenerative feedback to transistor Q4.

(3) The output from transistor Q6 is applied through coupling capacitor C5 to the base of paraphrase amplifier Q7 in the amplitude detector. Resistors R19 and R20 provide initial operating bias for transistor Q7. The amplitude detector operates exactly the same as the transmit carrier alarm circuits (para 5-136(2)).

(4) The amplitude detector output is applied through amplifier IN-10 to amplifier IN-9 and to the common alarm circuits in the input interface and common alarm module. As long as a carrier signal is detected by the amplitude detector, amplifier IN-10 conducts. The current flow through emitter resistor R45, transistor Q14, and collector load resistor R42 maintains amplifier IN-9 in a conducting state, thus preventing capacitor C9 from charging. Transistor Q11 is held cut off, thereby cutting off transistor Q12 (+15 volts applied to transistor Q12 base).

With transistor Q12 cut off, -6 volts is applied to the common alarm circuits, so that the common alarm circuit is not activated (para 5-24*f*).

(5) When the receive carrier is lost or falls below a predetermined level (as set by REC CARRIER ALARM THRESHOLD control resistor 1A1R11), transistor Q9 of the amplitude detector does not conduct; therefore, the base of amplifier IN-10 is at -15 volts, cutting off transistor Q14. With transistor Q14 cut off, the base of amplifier IN-9 is connected to -15 volts, which cuts off transistor Q10 and allows capacitor C9 to charge. Diodes CR9 and CR11 serve as small dropping resistances when transistor Q11 is forward biased.

(6) REC CARRIER ALARM TIME control resistor 1A1R12 adjusts the time required (2 minutes or longer) for capacitor C9 to reach a potential sufficiently positive to be passed by diode CR11 to transistor Q11, causing transistor Q11 to conduct. With transistor Q11 conducting, a ground is applied to bias transistor Q12 into conduction, providing +6 volts to activate the common alarm circuit.

(7) Resistor R35 is the collector load resistor for transistor Q11, resistor R36 provides direct coupling between transistors Q11 and Q12, and resistor R37 is the collector load for transistor Q12.

(8) The alarm signal (+6 volts), inverted by amplifier IN-11, is applied to the external receive carrier alarm terminal 14 of terminal board TB1 as a ground (transistor Q13 conducting). If a no-alarm condition exists, the -6 volts at the Q12 collector holds transistor Q13 cut off, which provides a positive output that is clamped to +6 volts by diode CR12. Resistor R39 is the collector load resistor for transistor Q13.

5-15. Talk-Request Detector Timing Circuits
(fig. 8-15)

a. General. The talk-request detector timing circuits include an initial timer that when activated upon receipt of a receive carrier alarm times out after approximately 1 second (adjustable by TALK REQUEST DELAY control resistor 1A1R9). After timing out, the initial timer activates the window timer, which times out after

approximately 0.75 second (adjustable by TALK REQUEST WINDOW control resistor 1A1R10). If the receive carrier alarm is actually a talk request, with a duration of 1.5 second, both the initial timer and the window timer are allowed to time out, lighting the front panel TALK REQUEST indicator lamp.

b. Initial Timer.

(1) With a carrier signal being received by amplifier IN-16, the negative input holds transistor Q1 conducting, thereby applying a ground to the input of transistor Q2. Transistor Q2 therefore conducts and Prevents capacitor C1 from charging. Diode CR2 is reverse-biased and holds transistor Q3 cut off, so that +15 volts is applied to the base of transistor Q4 keeping transistor Q4 cut off.

(2) Resistors R2 and R3 provide initial bias for transistor Q1, and resistors R4 and R5 form the dc coupling circuit for transistor Q2. Diode CR1 provides the emitter resistance, and resistor R6 is a collector load resistor. Diode CR2 and resistor R8 establish a positive feed through voltage level for transistor Q3, resistor R9 is the collector load resistor, and resistor R10 provides dc coupling between transistors Q3 and Q4.

(3) When a talk-request (or carrier alarm) condition occurs, a ground is applied, through pin H, to amplifier IN-16 and to diode CR6 of AND gate GAD-3. The ground passed by diode CR6 cuts off amplifier IN-18, which does not affect bistable FFB-1. However, the ground fed to amplifier IN-16 cuts off transistor Q1; consequently, transistor Q2 is cut off, allowing capacitor C1 to charge toward +15 volts through DELAY control resistor 1A1R9.

(*a*) If the alarm or talk-request signal persists for longer than 1 second (determined by resistor 1A1R9), the charge built on capacitor C1 is passed through diode CR2, biasing transistor Q3 into conduction. This action causes transistor Q4 to conduct and supply a positive collector potential to transistor Q7 in the window timer, and a positive input to transistor Q5 in the window timer.

(*b*) If the alarm condition does not remain for approximately 1 second, the circuits are reset to the original no-alarm condition ((1) above), and capacitor C1 discharges through conducting transistor Q2.

c. Window T7imer.

(1) Initially, in the no-alarm condition, transistor Q5 is conducting so that transistor Q6 conducts; this action prevents capacitor C2 from charging and transistor Q7 is held cut off. Circuit component functions for the window timer are essentially the same as for the initial timer (*b*(2) above).

(2) Approximately 1 second after an alarm condition occurs, collector supply voltage is applied to transistor Q7 from the initial timer (b(3) above). The positive voltage applied to transistor Q5 cuts off transistor Q5; consequently transistor Q6 is held cut off, allowing capacitor C2 to charge toward +15 volts through TALK REQUEST WINDOW control resistor 1A1R10. When capacitor C2 charges sufficiently (in approximately 0.75 second, as determined by TALK REQUEST WINDOW resistor 1A1R10), transistor Q7 conducts, placing a ground on the input of amplifier IN-17, to cut off transistor Q8. If the alarm signal is actually a talk-request, the positive input to diode CR6 of AND gate GAD-3 is removed after 1.5 second. With diode CR5 reverse biased by the -15 volts applied from amplifier IN-17, AND gate GAD-3 is inhibited, allowing amplifier IN-18 to conduct (due to current flow through resistors R22, R23, and R24). With transistor Q9 conducting, a positive input transition (-15 volts to ground) is applied through coupling capacitor C4 and diode CR7 to trigger bistable FFB-1; this action turns off transistor Q11, which in turn causes transistor Q12 to conduct and apply a ground to light the TALK REQUEST lamp.

5-16. Demodulator Circuits

(fig. 8-13)

a. The demodulator circuits consist of two identical limiting amplifier circuits, each comprising an operational amplifier, a feedback circuit and a shaper, several feedback amplifiers used for impedance matching, nonsaturating amplifier NSA-1, a 6-volt clamp, and a discriminator circuit. Input fsk signals are applied from the receiver filter to amplifier AM-5, an emitter follower. Resistors R1 and R3 form an input signal voltage divider, resistor R4 is a de collector limiting resistor, resistor R5 is the emitter load resistor, and resistors R68 and R69 are supply-voltage limiting resistors. Capacitors C14 and C15 are high-frequency bypass capacitors for the +15 volts power supply circuits. The output of amplifier AM-5 is coupled to an operating amplifier through a coupling network composed of resistor R6 and capacitor C1, *c* below, and also through coupling resistor R29 to amplifier AM-6, *b* below.

b. Input fsk signals from emitter follower Q9 are coupled through coupling resistor R33 to the receive discriminator, which provides a phase shift of 90°for the carrier center frequency of more than 90°for the space frequency, and of less than 90°for the mark frequency. The received discriminator output is applied to cascade impedance-matching amplifier AM-7 and AM-8. The output from AM8 is fed through a coupling network (resistor R39 and capacitor C7) to the operational amplifier (*c* below).

c. The limiting amplifier circuits are identical; therefore, only one (using transistors Q2 and Q3) is described below.

(1) Operational amplifier. Transistors Q2 and Q3 form a nonsaturating differential amplifier. Input signals applied to transistor Q2 cannot overdrive the stage, because the voltage developed across common resistor R9 (the input signal through transistor Q3) provides a degenerative effect on both transistors. The output from transistor Q3, inverted by transistor Q4, is applied to emitter follower Q5, which supplies enough drive-signal to the feedback circuit ((2) below). Resistor R7 and capacitor C2, and resistor R10 and capacitor C5 form a shift network for transistors Q2 and Q5, respectively; each network prevents a phase shift in the signals when the stage is changing operating levels.

Resistor R11 is the collector load for transistor Q3, resistor R12 is the base grounding resistance, and resistor R15 is the collector load for transistor Q4. Resistor R16 is a collector dc limiting resistor, and resistor R17 is the emitter load resistor for transistor Q5.

(2) Feedback circuit. Diodes CR1 and CR2 are negative breakdown diodes that conduct when the output voltage of transistor Q5 reaches a sufficiently negative level; diodes CR3 and CR4 are positive breakdown diodes that conduct when the output of transistor Q5 reaches a sufficiently positive level. Capacitor C3 provides a high-frequency feedback to transistor Q2, and resistor R70 provides a discharge path for the capacitor. Resistors R13 and R14, with capacitor C4, provide for low-frequency feedback to transistor Q2. The feedback circuits supply equal amounts of feedback for the low-frequency mark signal and the high-frequency space signal, so that the average dc output applied to the shaper circuit (through coupling resistor R18 and coupling capacitor C6) is as close to 0 volt as possible. The shaper, a high gain amplifier, provides sharp leading and trailing edges of the input signal. Resistor R20 is a collector load resistor, resistor R19 is the base resistor, and diode CR5 acts as a shunt limiter. The output of each shaper is applied to the phase detector (*d* below).

d. The phase detector, a nonlinear exclusive OR circuit, combines the original fsk input signals with the phase-shifted input. signals from the receive discriminator. The two carrier signal frequencies are identical, but 90° out of phase; therefore, the phase detector provides an output frequency that is twice the carrier frequency, with a 50-percent duty cycle. Because mark frequencies occur with less than 90° phase shift between them, the output duty cycle is greater than 51 percent. Space frequencies occur with more than 90°phase shift between the output; therefore, the duty cycle is less than 50 percent. This changing duty cycle produces an output sinusoidal voltage that varies above and below the average dc level

(approximately 0 volt), which is applied to the post detection filter circuits in receive discriminator filter FL3.

e. The post detection circuits remove the doubled carrier frequency and apply the changing dc voltage (positive for mark, and negative for space) to differential amplifier NSA-1 (Q17 and Q18.), where the other input is a reference from BIAS ADJ resistor 1A1R13. The sinusoidal recovered data applied to transistor Q17 is also coupled to the emitter of Q18 through emitter resistor R60. As the input voltage of transistor Q17 becomes more positive (above ground), the inverted output also increases (more negative) while, at the same time. the output of transistor Q18 becomes more positive (due to increased reverse bias on transistor Q18). Since both outputs are applied simultaneously to the 6-volt clamp circuit, the net effect is a constant positive output level during the mark bit. When the input signal through transistor Q17 becomes more negative (below ground),the inverted output becomes more positive; at the same time, the output of transistor Q18 becomes less positive, thereby, maintaining the output at a constant negative level during the space input bit. Thus, NSA-1 converts the sinusoidal input data signal to a square wave output data signal. Resistors R57 and R58 are the collector load resistors. Diodes CR15 and CR16 prevent the collector voltage from going higher than +6 volts.

f. The output signal levels from amplifier NSA-1 are applied, through the external connector, to 6-volt clamp transistor Q19. Diodes CR17 and CR18 maintain the output level between ground and -6 volts, respectively. Resistor R62 is the 6-volt dropping resistor when transistor Q19 conducts, resistor R6.3 is a collector load resistor, and resistors R64 and R65 form a voltage divider to set the operating voltage for BIAS ADJ resistor 1A1R13.

5-17 Dual Output Polar Driver Circuits

(fig. 8-10)

a. General. The timing output polar driver circuits consist of two identical groups of shaping and amplifying circuits. Risetime and falltime shaper No. 1 and linear amplifiers PDA-1 and PDA-2 provide corrected receive output timing signals; risetime and falltime shaper No. 2 and linear amplifiers PDA-3 and PDA-4 provide uncorrected transmit timing output signals. Only the first group of circuits is described in detail below.

b. Risetime and Falltime Shaper. Timing signals are applied to amplifier Q1 of risetime and falltime shaper No. 1 through a biasing network (resistors R1, R2, and R3). A 6-volt level input causes transistor Q1 to conduct, and a ground level input cuts off transistor Q1. The output square wave from transistor Q1 varies between ground and -15 volts. Resistor R4 is the collector limiting resistor, and resistor R5 is the collector load resistor for transistor Q1 and the emitter coupling resistor to transistor Q2. Transistors Q2 and Q3 form a grounded-base, complementary symmetry polar amplifier. With transistor Q1 conducting, ground is applied to cut off transistor Q2, allowing capacitor (,5 to charge to approximately +6 volts through conducting transistor Q3. With transistor Q1 cut off, the -15 volts applied to transistor Q2 emitter biases transistor Q2 into conduction. Capacitor C, discharges and then charges to approximately -6 volts through transistor Q2. Since transistor Q2 and Q3 each present the same high impedance to the charging of capacitor C5, the voltage across capacitor C5 is almost a perfect ramp, ranging linearly from +6 to -6 volts, in approximately the 27 microseconds required by the external equipments to which the timing signals are applied. Resistor R6 is the emitter dropping resistor for transistor Q3. Transistor Q4 amplifies the input signal and applies it to linear amplifiers PDA-: 3 and PDA-4. Resistor R7 is the collector load resistor, and diode CR2 clamps the collector of transistor Q4 to -6 volts when transistor Q4 is cut off.

c. Amplifier PDA-3. Amplifiers PDA-3 and PDA4 are identical circuits; therefore, only amplifier PI)A-, is described in detail. Amplifier PDA-3 consists of constant-current source amplifier Q6 and current-switching amplifier Q5, connected in a common-base configuration for maximum gain and minimum distortion. Transistor Q5 is essentially an emitter follower the output of which follows the input signal; transistor Q6 is the emitter load for transistor Q5. Since the two transistors are in series, their common current varies as the input signal applied to transistor Q5 varies. The action of the two transistors provides

a linear output signal to the timing output terminals. Diode CR1, in series with the base-emitter junction of transistor Q5, compensates for the diode characteristics of the junction. Diode CR3 limits transistor Q5 collector voltage to +6 volts; resistors R8 and R9 provide for proper biasing of transistor Q5; and resistors R10 and R11 provide for proper biasing of transistor Q6.

5-18. Delay Equalization Circuits

a. General. The delay equalization circuits provide varying amounts of delay for the different input frequencies of the received fsk signals, so that the output from the delay equalization circuits contains the same amount of delay and, hence, no delay distortion for all frequencies in the appropriate channel received. The schematic diagram shown in figure 8-25 represents the circuits employed in the MX-7379/G only, employing a separate delay equalizer PC card (PC80034230; assy A25A3) and switching circuit; for all other MX-73(*)/G's, the PC card is not used. For the MX-7380/G, MX-7383/G, and MX-7384/G, MX-7385/G, a switch selection circuit is provided to vary the amount of delay (A, fig. 8-26). For the MX-7372/G through MX7378/G, and MX-7381/G and MX-7382/G (B, fig. 8-26), no selection is provided; only a fixed amount of delay is available. Discussion of delay equalization used with the MX-7379/G is given in *b* below. Operation of the other types is self-evident when analyzed from the overall delay equalization discussion given in *b* below.

b. Circuit Operation (fig. 8-25).

(1) The received input signals are applied to paraphase amplifier Q1, which provides two outputs that are equal in frequency and amplitude and 180° out of phase with each other. Capacitor C1 is the coupling capacitor, and resistors R1 and R2 provide operating bias for transistor Q1. Resistor R3 is the emitter load resistor, and resistor R4 is the collector load resistor. Resistor R12 and capacitor C5 and resistor R13 and capacitor C6 provide additional filtering of the dc power supply voltages.

(2) Output from transistor Q1 emitter is applied, through a delay capacitor in the receive filter, to impedance-matching emitter follower Q2. With EQUALIZER switch S1 at OUT, the delay capacitor is shorted out so no delay is introduced into the received signal. With EQUALIZER switch S1 at COMP, the output. from the collector of transistor Q1 (through coupling capacitor C2 and resistor R5, through resistor R8) is applied to transistor Q2; at the same time, the output from the emitter of transistor Q1 is applied through the delay capacitor in the receive filter to transistor Q2. This parallel arrangement provides a small amount of delay over a relatively wide frequency band. With EQUALIZER switch S1 at ADJ, DELAY ADJ resistor R6 is substituted for fixed resistor R8, providing an adjustment of the delay range.

(3) When FREQ switch S2 is at B, a parallel-tuned circuit is added, in parallel with the delay circuits described in (1) and (2) above; this arrangement provides a larger amount of delay over a narrower frequency band.

(4) The delayed signal is applied through transistor Q2 to another delay circuit that is identical with that described in (1), (2), and (3) above. The delayed signal, amplified by transistor Q4, is applied through coupling capacitor C4 to the remainder of the receive circuitry. Resistor R10 is the emitter-biasing resistor, and resistor R11 is the collector load resistor for transistor Q4.

Section IV. LOGIC ANALYSIS

5-19. Transmit Data
(fig. 8-5)

a. Input data is applied through ORDER WIRE SEND jack 1A1J1 (no plug inserted) from the TRANSMITTER DATA INPUT terminals and INPUT SELECT switch 1A1S5 (switch at DATA) to differential amplifier DIA-1. Differential amplifier DIA-1 provides two output signals that are 180°out of phase with each

other to AND gates GAS-1 and GAS-2 in the common alarm module (para 5-24) and to AND gates GAI-1 and GAI-2 in the crystal oscillator and oven regulator module.

(1) When the transmit data input is in a mark condition, differential amplifier DIA-1 output (negative) enables AND gate GAI-1, and the positive output inhibits AND gate GAI-2. Thus, the output of mark oscillator OSC-1 is fed through AND gate GAI-1 and through the hidden OR gate to inverter IN-1 in the MX73(*)/G countdown assembly A18A2-A32A2.

(2) When the transmit data input is in a space condition, differential amplifier DIA-1 output enables AND gate GAI-2, and inhibits AND gate GAI-1. Thus, output of space oscillator OSC-2 is applied through AND gate GAI-2 and the hidden OR gate to IN-1, Diode A16CR1 maintains the oscillator output signal level between 0 and -6 volts.

b. The frequency-determining module (fdm) countdown assembly may contain three bistables (fig. 8-24), or it may use only one or two bistables (figs. 8-22 and 8-23, respectively, depending on the output mark frequency and space frequency desired for the particular configuration. Where an fdm countdown assembly is not used, the mark and space frequencies are routed through pin 20 of connector A18P1-A32P1 directly to the 64 divider module. (Pin 20 is opened when an MX-73(*)/G countdown assembly is used.)

c. The countdown assembly and the ,64 divider assembly count down the mark frequency and the space frequency from mark oscillators OSC-1 and space oscillator OSC-2, respectively, to the required channel frequencies. A positive input trigger is required by each bistable FFC-1 through FFC-9. The output square wave of bistable FFC-9 (either at the mark or space frequency) is applied to phase-splitting amplifier PSA-1, which provides a polar square-wave output to transmit filter FL2. Transmit filter FL2 converts the square-wave input to a vf sine-wave signal and applies it from pin 7 to amplifiers AM-3 and AM-4 in the 64 divider module. Amplifiers AM-3 and AM-4, together with an attenuation pad in transmit filter FL2. allow for enough filter bandwidth at all operating frequencies, particularly at the higher channels. The final vf output signal from the transmit filter (after any necessary attenuation) is applied from pin 3 to the output amplifier circuit in the transmit output and carrier alarm module (para 5-24) through OUTPUT LEVEL ADJ resistor 1A1R6. The vf signal from the output amplifier circuit is coupled through transformer 1A1T2 to the BALANCED XMTR CARRIER OUTPUT terminals at the rear of the unit. OUTPUT switch 1A1S7 controls the output impedance; with the switch at 600Ω, resistor R38 and diodes CR12 and CR13 are placed across the secondary of transformer 1A1T2 to provide an output impedance of 600 ohms. With the switch at 50KΩ, the output impedance is 50,000 ohms.

5-20. Send Timing

Bit-timing signals are supplied to the external transmitting equipment in either phase (strap selected). Initial timing signals (clock) may be provided by an internal 1.2288 megacycle (mc), crystal-controlled oscillator (*a* below) or may be supplied from an external source at bit-rate (*b* below).

a. Internal Clock. Output of the 1.2288-mc, crystal oscillator (fig. 8-5) is applied through inverters IN-20 (which isolates the crystal oscillator) and IN-21 (which provides the proper phase of the oscillator signal; to a three-stage binary counter. Bistables FFC-13, FFC-14, and FFC-15 divide the 1.2288-mc input frequency by 8, to provide timing signals of 153.6 kilocycles (kc) to the variable-control oscillator module. With the variable-control oscillator module strapped for INT CLOCK, the 153.6-kc signal from bistable FFC-15 is inverted by inverter IN-15, and applied to a second three-stage binary counter (bistables FFC-10, FFC-11, and FFC-12). Output from each bistable, plus the output of FFC-15, is applied to separate contacts of BAUD RATE switch 1A1S2, which selects the output of one of the bistables, depending on the operating rate desired. With BAUD RATE switch 1A1S2 at 1200,. the 153.6-kc signal from bistable FFC-15 is applied to the 128 divider-A module. At 600, 300, and 150 BAUD RATE switch 1A1S2 selects and applies the output of FFC-10(76.8kc), FFC-11 (38.4 kc), and FFC12 (19.2 kc), respectively, to the 128 divider-A module. The selected frequency from BAUD

RATE switch 1A1S2 is applied to inverter IN-22 and then to a seven-stage binary counter (bistables FFC-16 through FFC-22) that divides the selected input frequency by 128, providing an output timing signal equal to the operating bit-rate. Inverter IN-22 assures proper phasing of the input signal to bistable FFC-16. The set (1) output of bistable FFC-22 is applied through connector XA5, pin J, to risetime and falltime shaper No. 2 in the dual output polar drivers module. The output of risetime and falltime shaper No. 2, which provides sharp leading and trailing edges of the timing signal, is applied to polar driver amplifiers PDA-3 and PDA-4. Each amplifier provides a square wave, polar output bit-timing signal to the transmitting equipment. The two outputs, in phase with one another, accommodate external transmitting equipments that require either phase (strap selectable) of bit-timing signals.

b. External Clock.

(1) The external clock timing signal is applied to the modem at a bit-rate, which is incompatible with the timing requirements of the MD-674(P)/G. Since the timing circuits require a clock signal of exactly 128 times the bit-rate, an internal variable-control oscillator (VCO) is used to generate the necessary clock signals of 153.6 kc. A phase lock loop automatically adjusts the output frequency of the VCO to exactly 128 times the operating rate of the applied bit-timing signal. The VCO frequency (approximately 153.6 kc) is applied to the 128 divider-A module through BAUD RATE switch 1A1S2 as described in a above. Two outputs, 180 out of phase with one another, at the selected bit-rate are applied to OR gates GOA-4 and GOA-5. The second input to OR gates GOA-4 and GOA-5 is externally applied at a bit-rate equal to the clock signal. The external timing signals are fed to differential amplifier DIA-2, which produces two output signals 1800 out of phase with each other. Differential amplifier DIA-2 also prevents any noise signals from affecting the MD-674(P)/G when the external timing signal is removed.

(2) The VCO provides a bit-timing signal from the 128 divider-A module, 90° out of phase with the incoming bit-timing signal. In this case, the VCO frequency is phase locked to a frequency that provides a clock signal (to the 128 divider-A module) exactly 128 times the incoming bit-timing signal. If the VCO frequency is not correct, its frequency is appropriately adjusted by OR gates GOA-4 and GOA-5 and AND gate GAI-4 (which together make up an exclusive OR circuit).

(3) Assuming the in-phase condition, the input bit-timing signal is applied to differential amplifier DIA-2, providing two outputs (A and B, fig. 5-8). The generated bit-timing signal from the 0 output of FFC-22 (fig. 8-5) in the 128 divider A module (C, fig. 5-8), with an output from differential amplifier DIA-2 (A, fig. 5-8), produces a negative output from GOA-4 (E, fig. 5-8) whenever the two inputs (A and C, fig. 5-8) are negative and in coincidence. Output of GOA-5 is also negative whenever its two inputs (B and D, fig. 5-8) are negative and in coincidence. Output of GOA-4 and GOA-5 are applied to AND gate GAI-4 which required two positive inputs (E and F, fig. 5-8) to provide a negative output. The resultant output from GAI-4 (G, fig. 5-8) is twice the bit-rate and is symmetrical, resulting in a constant average dc voltage that is applied to maintain the VCO frequency in phase.

(*a*) If the VCO were not in phase with the input timing signal, the output of FFC-22 (C, fig. 5-8) in the 128 divider-A module (bit-timing) would not be exactly 90° out of phase with the input timing signal. Waveforms H and J, figure 5-8, indicate a generated bit-timing signal that is early with respect to the input bit-timing signal (A and B, fig. 5-8). Because of the coincidence required by GOA-4, GOA-5, and GAI-4 (described above), the output of GAI-4 (M, fig. 5-8) is no longer symmetrical, resulting in application of a lower

average dc voltage to the VCO. This lower dc voltage causes the VCO to *slow down* or decrease its frequency enough to cause the generated bit-timing signal (from FFC-22) to occur a little later, thus moving toward the phase-lock condition of 90° out of phase with the input timing signal. This operation continues until the phase-lock condition between the generated clock and the input timing signal is achieved.

(b) Waveforms N and P, figure 5-8, indicate a generated bit-timing signal that is late with respect to the bit-timing input (A and B, fig. 5-8). This results in the output of GAI-4 (Q, fig. 5-8) being positive longer than it is negative, resulting in a higher average

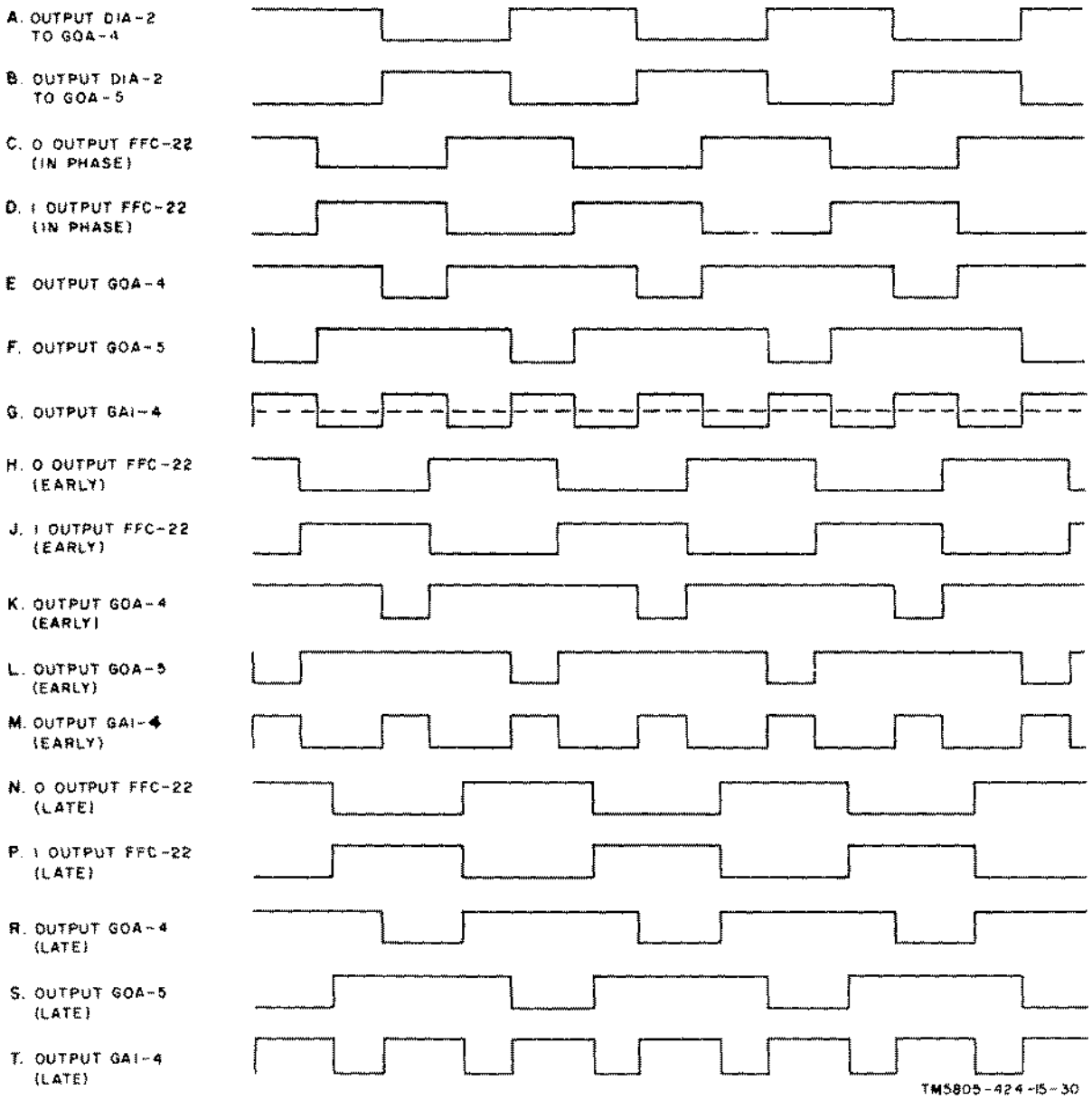


Figure 5-8. Phase-lock loop, timing waveforms.

dc voltage applied to the VCO. This higher dc voltage increases the VCO, causing the bit-timing signal from FFC-22 to occur sooner, and moving its transitions closer to the 90° phase-lock condition. Thus, the generated clock signals from the VCO are adjusted automatically so that its output frequency, applied through BAUD RATE switch 1A1S2 to the 128 divider-A module, is always exactly 128 times the input bit-timing signal frequency.

5-21. Receive Timing

a. Add-Subtract Control Logic. Clock signals, at 128 times the baud rate as selected by BAUD RATE switch 1A1S2 (fig. 8-5), are applied through inverter IN-22 (128 divider-A module) to inverter IN-23 in the add-subtract logic module. The timing signals are inverted, and the positive transitions (A, fig. 5-9) are applied to bistable FFG-1, in the 128 divider-B module (fig. 8-5). Bistable FFG-1 divides the input frequency by 2 (B, fig. 5-9) providing a positive trigger to alternate sides of bistable FFD-5, through AND gates GAS-5 though GAS-6 (*b* below). Bistables FFC-23 through FFC-27 (fig. 8-5) form the remainder of the seven-stage countdown chain (D, through H, fig. 5-9), providing an output timing signal equal to the baud rate (bit-time). To minimize distortion of the received data signal (due to a phase difference between the transmit timing and the receive timing), the receive timing clock is synchronized with the data clock, by comparing the receive bit-timing output from bistable FFC-27 with the received data transitions.

(1) Assuming that the receive clock is late (timing signal transitions occur later than the receive data transitions), the positive data-bit (K, fig. 5-9) allows the 128 times baud timing signal to set bistable FFD-1 clear side (fig. 8-5), providing a negative output from FFD-1 (L, fig. 5-9). This negative output has no effect on subsequent circuitry. When the inverted data signal (J, fig. 5-9) is applied to the clear input steering AND circuit of bistable FFD-1 (fig. 8-5), the positive timing trigger (A, fig. 5-9) produces a positive output from the clear side of FFD-1 (L, fig. 5-9) that is applied to the clear (C input of bistable FFD-2 (fig. 8-5) and FFD3. With the positive output of FFC-27 (H, fig. 5-9) in coincidence with the positive output of FFD-1 (L, fig. 5-9). FFD-2 is cleared providing a positive output at the 0-output line (fig. 8-5) and a negative output at the 1-output line. The positive output at the 0-output line is fed back to the set (S) input steering circuit, where the next positive timing pulse (A, fig. 5-9) sets FFD-2, thus a negative pulse was provided (M, fig. 5-9) from the 1-output line of FFD-2; this pulse advances the receive clock. The positive output of FFD-1 (fig. 8-5), applied to FFD-3, clears FFD-3, providing a negative output at the 1output line (M, fig. 5-9). The positive output at the 0-output line, fed back to the input steering circuit, allows the next positive timing pulse (A, fig. 5-9) to set FFD-3 therefore, a negative pulse appeared at the 1-output line of FFD-3. This pulse retards the receive clock.

(2) Assuming that the receive clock is early (timing signal transitions occur sooner than the data-transitions), bistable FFD-1 (fig. 8-5) provides a positive output (L, fig. 5-9) as described in (1) above. This positive output clears bistable FFD-3 (fig. 8-5), which provides a negative output pulse (N, fig. 5-9) as described in (1) above. With the output of bistable FFC-27 supplying an early timing transition (P, fig. 5-9), no coincidence is possible between the positive output of FFC-27 and the inverted data signal (J, fig. 5-9). As a result, bistable FFD-2 is never cleared and its 1 output remains in a set or positive condition, so that no negative pulse is produced to advance the receive timing clock.

b. Clock Correction. Correction of the receive clock is accomplished in the 128 divider-B module. The 1-output from bistable FFD-3 (fig. 8-5) in the add-subtract control logic module is applied to AND gates GAD-6 and GAD-7 which require two positive inputs to be enabled and provide a positive output. With the FFD-3 output line 1 in a positive condition (N, fig. 5-9), AND gates GAD-6 or GAD-7 can be enabled, depending on the state of bistable FFG-1. Assuming bistable FFG-1 (fig. 8-5) is in a set state; the 1-output line is positive and the 0-output line is negative. The negative output of the 0-output line inhibits AND gate GAD-6 providing a negative input to the C input steering circuit; the positive output at the 1-output line enables GAD-7 which provides a positive input to the S-input steering circuit. Under these conditions. the next positive clock timing signal from inverter IN-23, in the add-subtract control

logic module clear bistable FFG-1. The resultant positive output at the 0-output line now enables AND gate GAD-7, while the negative output at the 1-output line inhibits AND gate GAD-6; thus the S-input steering circuit passes the next positive clock timing pulse to reset bistable FFG-1. Bistable FFG-1 is alternately set and reset by successive positive transitions of the clock signal, thus providing a 2-to-1 signal division. The 1-output of bistable FFG-1 is applied to AND gates GAS-5 and GAS-6, which act as the steering inputs to bistable FFD-5. The positive-going transitions of bistable FFG-1 output line 1 (B, fig. 5-9) are alternately applied through AND gates GAS-5 and GAS-6 thus alternately setting and resetting bistable FFD-5 by successive positive-going transitions from bistable FFG-1. The output of bistable FFD-5 is applied to bistable FFC-23 and subsequently to the remainder of the seven-stage countdown chain, resulting in an output (from bistable FFC-27) that is equal to the bit-time.

(1) Assuming that bistable FFC-27 output bit-timing signal is early (P, fig. 5-9), the negative output produced by bistable FFD-3 (fig. 8-5) inhibits both AND gates GAD-6 and GAD-7. The resulting negative output from each gate inhibits both input steering circuits to bistable FFG-1. Thus, the next positive clock pulse cannot trigger bistable FFG-1, so the bistable remains in the same state for two clock counts. As a result, the time required to trigger bistable FFC-27, which provides the negative output transition (P, fig. 5-9), is lengthened by one count. In this case, 129 input counts, rather than 128, are required to trigger bistable FFC27; therefore, the bit-timing transition from bistable FFC-27 is made to move toward the data transition (J, fig. 5-9). This action continues, with one clock pulse being deleted for each cycle (128 actual inputs) of the bit-timing signal, until the bit-timing transition from bistable FFC-27 is in line (synchronized) with the data transition.

(2) Assuming that bistable FFC-27 output bit-timing signal is late (H, fig. 5-9), one clock pulse is prevented from triggering bistable FFG-1 (fig. 8-5) as described in (1) above; as a result, one count is lost in the timing chain, thereby retarding the receive clock by one count. However, with an early output from bistable FFC-27, a negative output is provided by bistable FFD-2 (a (1 above) which is applied to AND gates GAS-4 and GAS-7. Depending on the state of bistable FFD-5, one of these gates is enabled at the trailing edge (positive transition) of the bistable FFD-2 output, providing a positive pulse to trigger bistable FFD-5. Triggering the second bistable in a counting chain advances the counting sequence by two (since two inputs from the first bistable in the counting chain are normally required). Because one clock pulse is inhibited from bistable FFG-1 at the same time that bistable FFD-5 is triggered, the net effect is to advance the overall count by one, thus decreasing the time required to trigger bistable FFC-27 and moving the bit-timing transition (H, fig. 5-9) toward synchronism with the inverter data transition (J, fig. 5-9).

(3) A count is always subtracted from the receive clock once each cycle; therefore, the bit-timing signal from bistable FFC-27 at synchronism is alternately late and early by one count, resulting in a 2-count jitter. This amount of jitter has a negligible effect on the overall timing of the data signal. The corrected receive bit-timing signal from bistable FFC-27 (fig.

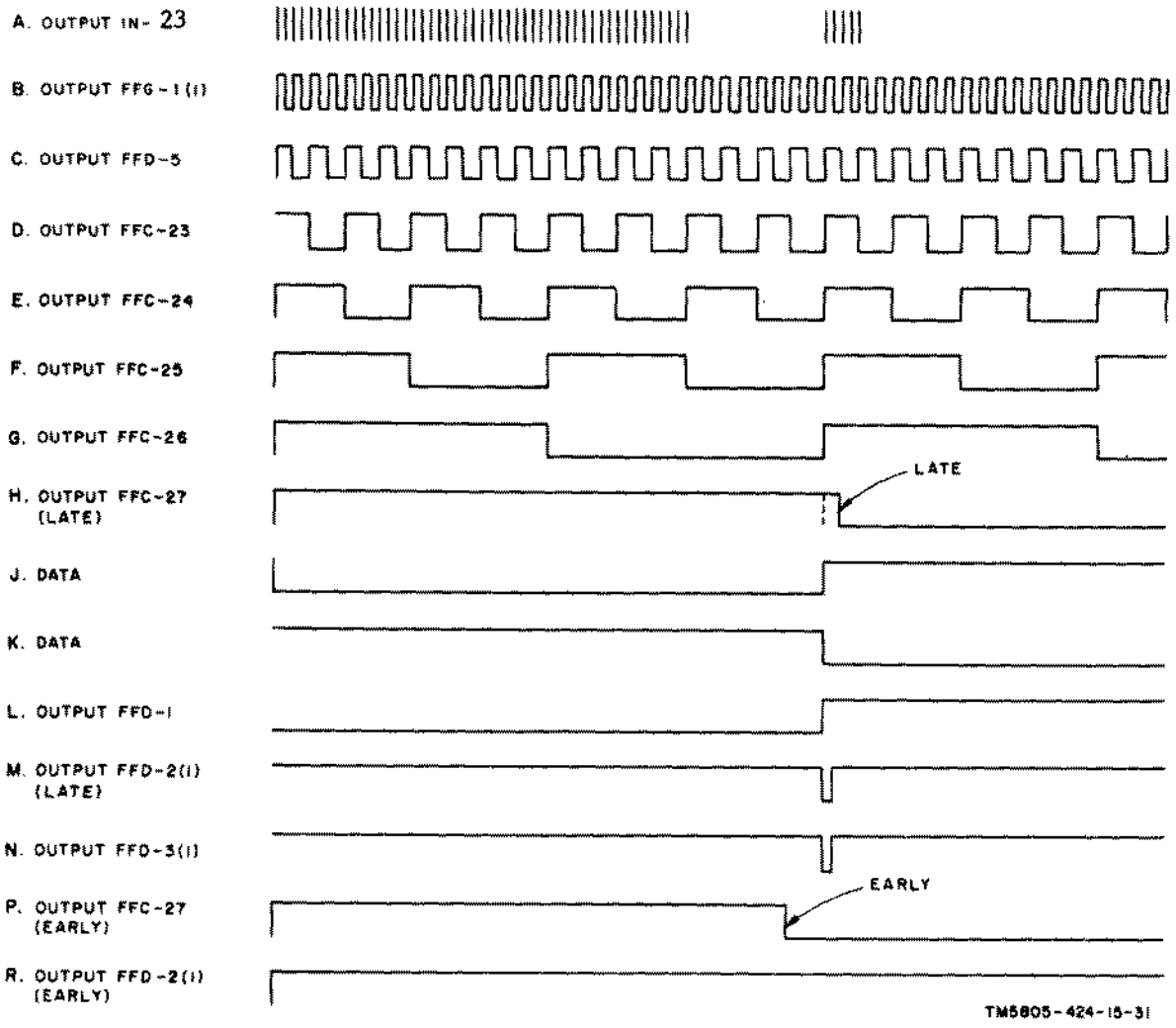


Figure 5-9. Receive timing add-subtract control logic waveforms.

8-5) is applied to the dual output polar drive module, where either phase of the output from bistable FFC-27 is strap-selectable. Risetime and falltime shaper No. 1 provides a squared bit-timing signal to drivers PDA-1 and PDA-2, which provide for two corrected bit-timing signal outputs to the external receiving equipment. The bit-timing signal from the 0-output line of bistable FFC-27 is also applied to the receive data output module, where the received data signal is retimed for application to the external receiving equipment (para 5-22).

5-22. Receive Data

(fig. 8-5)

a. Received fsk signals are coupled from the BALANCED REC CARRIER INPUT terminals, through isolation transformer 1A1T3, to first input amplifier Q1. INPUT switch 1A1S8 connects resistor A9R44 across the primary of transformer 1A1T3 for operation with a 600-ohm input line. First input amplifier Q1 provides a reshaped signal to the delay equalizer (used only with MX-7379/G) and through resistor A9R3 to receive filter FL1. The delay equalizer assembly provides equal delay of the mark and space frequencies in the fsk input

signal in the high 1,800cycle-per-second (cps) channel; for all other channels, this delay equalization is unnecessary.

(1) With delay equalizer assembly A25A3 in use, pin 26 of the MX-73(*)/G module is open and the input signal is passed through the delay equalizer module to second input amplifier Q2, Q16.

(2) If the delay equalizer assembly is not used, the input signal from resistor A9R3 is routed direct to second input amplifier Q2, Q16.

b. Second input amplifier Q2, Q16, a constant-current generator, matches the input characteristics of receive filter FL1, which filters out all undesired frequencies and provides only the correct channel frequencies (including the mark and space frequencies) to amplifier AM-5 in the demodulator module (*c* below). The input signal is also applied through resistor A8R2 to third input amplifier Q15 in the receive input and carrier alarm module for operation of the receive carrier alarm signals (para 5-24).

c. The output of amplifier AM-5 is applied through amplifier AM-6 to receive discriminator FL3 and to demodulator Q2-Q8, Q12-Q16.

(1) Receive discriminator FL3 demodulates the fsk input signals, producing a dc output signal that contains the original transmitted data information. At the mark frequency, the phase shift from the discriminator is more than 900; a 90°shift is produced at the center frequency. At the space frequency, the phase shift is less than 90°. The shifted output signal from the discriminator is applied through isolation amplifiers AM-7 and AM-8 to demodulator Q2-Q8, Q12-Q16.

(2) Demodulator Q2-Q8, Q12-Q16 compares the fsk signals from amplifiers AM-5 and AM-8. Phase relationships of the two signals applied to the demodulator vary (on either side of 90°), causing the demodulator output pulse to vary in duty cycle. The average dc level at the output of the demodulator represents the recovered data signal.

d. The demodulator output is applied to post detection filter FL3, which blocks the carrier center frequency and applies the resultant dc signal (containing the mark and space information) to nonsaturating amplifier NSA-1 which acts as a slicer, to limit output signal levels. Polar output signal from nonsaturating amplifier NSA-1 is applied to 6-volt clamp Q19 that produces a 0-volt to a -6 volt DC NEUTRAL signal to AND gate GAI-3 in the receiver data output module.

e. The output of AND gate GAI-3 is fed to AND gate GAS-3, amplifier IN-12, and bistable FFA-1.

(1) AND gate GAI-3 inverts the input data signal when a talk-request signal (para 5-23) is not applied to its second input. If a talk-request signal is applied to its second input, the output remains at a constant negative level for the duration of the talk-request signal, thus inhibiting all subsequent circuits. In normal operation, a positive output from AND gate GAI-3 triggers timing bistable FFA-1. When the bit-timing signal is applied in coincidence, negative output from AND gate GAI-3, inverted by amplifier IN-12, is applied as a positive pulse to the S (set) input of bistable FFA-1. Thus, bistable FFA-1 output is generated in accordance with the corrected bit-timing signal from the 128 divider-B module (para 5-21) and provides a retimed output data signal that is in synchronism with the master clock timing.

(2) The output of bistable FFA-1 is applied to AND gate GAD-2 and to strap terminal 3 at the input of the risetime and falltime shaper.

(*a*) If straps 3 and 4 are connected, a retimed (regenerated data signal is applied to the risetime and falltime shaper, which provides a sharply defined square-wave input for polar output data amplifier POD-1. Amplifier POD-1 supplies a polar output data signal with a +6volt mark bit, and a -6-volt space bit.

(*b*) If an unregenerated receive data output signal is desired, terminal straps 2 and 4 are connected so that recovered data is applied directly from amplifier IN-12 to the risetime and falltime shaper.

(*c*) Received data may be automatically switched from regenerated to nonregenerated through the talk-request facility as described in paragraph 5-23. If the data output signal is to be regenerated terminal straps 1 and 4 are connected together. In this case, AND gate GAD-2 is enabled and applies the regenerated signal from bistable FFA-1 through the hidden OR gate to the risetime and falltime shaper. If the data output signal is unregenerated, AND gate GAD-4 is enable and applies the recovered data signal

from IN-12 ungenerated by bistable FFA-1 through the hidden OR gate to the risetime and falltime shaper. Unregenerated output from amplifier IN-12 is also applied to AND gate GAS-4 for use with the no-transition receive alarm circuits (para 5-24).

5-23. Order-wire Circuit Operation (fig. 8-5)

a. Talk-Request Generation

(1) When TALK REQUEST switch 1A1S3 is depressed, a ground is applied through the hidden OR gate to amplifier IN-24 Amplifier IN-24 applies a ground output to trigger bistable FFF-1 and (through OR gate GOA-6) to bistable FFE-1. A remote talk-request signal (ground may also be used to initiate the talk request. (If this application is desired, terminals 1, 2, and 3 are connected together).

(a) With FFF-1 cleared the positive output from its 0-output line is applied to OR gate GOA-2 in the transmit output and carrier alarm module (inhibiting the transmit carrier alarm circuits) and to OR gate GOA-1 in the input interface and common alarm module (inhibiting the no-transition-send alarm circuitry).

(b) With FFE-1 cleared the positive output from its O-output line inhibits bistable FFC-8 in the transmit 64 divider module, thus inhibiting the transmit carrier. The negative output at the 1-output line of FFE-1 activates the 1.5-second delay; after 1.5 seconds, FFE-1 is set by the 1.5-second delay. The positive output at the l-output line of FFE-1 deactivates the 1.5second delay, and removal of the positive output from the O-output line of FFE-1 unblocks the transmit carrier. Thus, the carrier signal is interrupted for a period of exactly 1.5 seconds; this is interpreted at the other site as a talk request signal (b below). The transmit carrier alarm remains inhibited during the entire talk request mode of operation.

(2) When the order-wire mode of operation is no longer required, TALK REQUEST RESET pushbutton 1A1S4 is depressed, applying + 15 volts to bistable FFF-1, setting the bistable, and removing the positive inhibit level from OR gate GOA-2 (transmit carrier alarm circuits) and GOA-1 (NO-TRANSITIONSEND-ALARM circuits).

b. Talk-Request Detection.

(1) Under normal data operation, amplifier IN-16 is held on by the no-alarm output (-15 volts) of amplifier IN-10 in the receive input and carrier alarm module. Both timers are inactive, and bistable FFB-1 is in a set state with a high positive level output at its 1-output line, and TALK REQUEST indicator lamp DS3 is extingished.

(2) When a 1.5-second talk-request signal is received by the receive input and carrier alarm module, amplifier IN-10 assumes the alarm condition and provides a High Positive Level at its output (para 5-24). This High Positive Level cuts off amplifier IN-16. which activates initial timer Q2, Q3, Q4. The negative output of amplifier IN-16 inhibits AND gate GAI-3 which prevents receive data signals from being applied to the receive data output terminals. The initial timer times out a delay of approximately 1 second (adjustable by DELAY resistor 1A1R9). After the delay the positive output of initial timer Q2. Q3, Q4, is applied to the window timer Q5, Q6, Q7, (4 below) through resistor R11 to amplifier IN-17.

(3) Positive output from initial timer Q2, Q3, Q4 is inverted by amplifier IN-17, applying a negative input to NAND gate GAD-3. The positive talk-request signal (input to amplifier IN-161 maintains NAND gate GAD-3 in an inhibited condition, which provides a positive output that is inverted by amplifier IN-18 to a negative level that has no effect on bistable FFB1. However, when the talk-request signal is removed (after 1.5 seconds, both NAND gate GAD-3 inputs are negative. providing a negative output that clear bistable FFB-1 when inverted to a positive signal by amplifier IN-18. With bistable FFB-1 cleared a negative output is present on its 1-output line, and a positive output is present on its 0-output line. These outputs serve in automatic switching of timing bistable FFA-1 in the receive data output module (para 5-221. The negative output at the 1-output line of FFB-1 inverted by amplifier IN19, provides a ground to light TALK REQUEST indicator lamp DS3. The positive level at the 0-output line inhibits OR gate GOC-1 in the receive input and carrier alarm module, and OR gate GOA-3 in the receive data output

module. Therefore, the receive loss of carrier alarm circuits and the no-transition receive alarm circuits. respectively, are deactivated.

(4) When activated, window timer QS, Q6, Q7 times out an additional 0.75 second of delay (adjustable by TALK REQUEST WINDOW resistor 1A1R 101, resulting in a total delay (from the two timers approximately 1.75 seconds, slightly longer than the talk-request signal. After the delay, window timer Q5, Q6, Q7 provides a positive output (ground) that is inverted to a negative signal by amplifier IN-17 for application to NAND gate GAD-3. This high from the window timer for an additional 75 seconds, insures that NAND GATE GAD-3 is enabled to clear FFB-1 through IN-18 when the 1.5 seconds TALK-REQUEST signal is removed when a valid TALK-REQUEST is relieved.

(5) After order-wire circuit operation is concluded, operation of the TALK REQUEST RESET pushbutton provides + 15 volts to bistable FFB-1 The resultant positive output at bistable FFB-1 output 1 is inverted to a negative signal by amplifier IN-19, extinguishing the TALK REQUEST indicator lamp.

(6) If a true alarm condition exists at the input to amplifier IN-10, AND gate GAD-3 is held inhibited, providing a positive input to amplifier IN-18. This action prevents any reaction by bistable FFB-1 which is therefore held in a condition that prevents TALK REQUEST indicator lamp DS3 from being lighted during an alarm condition (which must last for more than 2 seconds).

5-24. Alarm Circuits (fig. 8-5)

a. General. Four alarm circuits sense loss-of signal transitions and loss-of-carrier signals. A common alarm circuit and an ALARM indicator lamp are activated when any of the four alarm conditions exists. External terminal connections are provided for connecting individual alarms that will light according to the actual single alarm condition that exists when the common ALARM indicator lamp is lighted. A no-transition alarm will be activated if signal transitions do not occur for a 5-second period. A carrier alarm will be activated if the carrier is interrupted longer than 2 seconds. Provisions are made to disable all alarm circuitry, by setting ALARM switch 1A1S6 to DISABLE.

b. No-Transition Send Alarm. The no-transition send alarm is activated if no data transitions are in the send circuits for 5 seconds or longer.

(1) Input data from amplifier DIA-1 is applied to AND gates GAS-1 and GAS-2. The two gates, working in conjunction, pass both the positive signal transitions and the inverted negative signal transitions (as positive transitions) to delay driver Q5, Q6, Q7. As long as positive pulses are applied (time between transitions is not greater than 200 milliseconds), delay driver Q5, Q6, Q7 remains inactive, providing a negative input that maintains 5second delay Q8 deactivated. The resultant positive output from 5-second delay Q8 is inverted to a negative level by amplifier IN-3 and applied to OR gate GOB-1. With no other alarm condition present, OR gate GOB-1 is inhibited *e* below), providing a low-level output that is inverted by amplifier IN-5. The resulting high-level (+15 volts) output from amplifier IN-5 holds ALARM indicator lamp 1A1DS2 in the *off* condition.

(2) If data transitions occur at intervals greater than 200 milliseconds but less than 5 seconds apart, delay driver Q5, Q6, Q7 provides a positive input to activate 5-second delay Q8. The next transition resets delay driver Q5, Q6, Q7 and 5-second delay Q8.

(3) If no transition is received after 5 seconds, 5-second delay Q8 times out, providing a low-level input to amplifier IN-3. The resultant high-level output from amplifier IN-3 enables OR gate GOB-I and provides a high-level output which, inverted by amplifier IN-5 provides ground to light ALARM indicator lamp 1A1DS2. The +6 volts from amplifier IN-3 allows amplifier IN-4 to conduct and apply a ground level to the NO TRANSITION ALARM SEND output terminal, to activate an external no-transition send alarm.

(4) The no-transition send alarm may be deactivated by applying a high-level input (+6 volts) through OR gate GOA-1; this action applies a steady positive level to delay driver Q5, Q6, Q7, keeping 5-second delay Q8 deactivated ((1) above). The positive input to GOA-1 may be

applied from ALARM switch 1AIS6 (DISABLE position), or from bistable FFF-I in the talk-request generator module when orderwire circuit operation is activated (para 5-231.

c. Loss-of-Transmit-Carrier Alarm. The loss-of-transmit-carrier alarm will be activated if the transmit-carrier output is interrupted for 2 seconds or longer.

(1) When the carrier signal is interrupted, the output of the transmit filter to OUTPUT LEVEL ADJ resistor 1A1R6 (transmit output and carrier alarm module) is removed. With no signal applied through XMIT CARRIER ALARM THRESHOLD resistor 1AIR14 (which presets the minimum signal level requirements before an alarm condition is detected), level threshold Q4, Q5 in the transmit output and carrier alarm module does not have an output. This drop in signal level is interpreted by IAM) Detector Q6-Q8 as an alarm condition. With no input to IAMI Detector Q6-Q8, a positive output is applied to activate 2-second delay Q9-Q 11.

(a) If the carrier level is restored before 2 seconds have elapsed, level threshold Q4, Q5 provides an output dc level to reset (AM) Detector Q6-Q8 and 2-second delay Q9-QII before any change in the output can occur.

(b) If the carrier level remains below the predetermined level (as determined by XMIT CARRIER ALARM THRESHOLD resistor 1A1R14), 2-second delay Q9-Q 11 times out and provides a high-level output to OR gate GOB-1, which lights ALARM indicator lamp 1AiDS2 (*b*(3) above). The output of the 2-SEC delay Q9-QII is also inverted by amplifier IN-8 and applied as a low-level (ground, in this case) alarm signal to the LOSS OF XMTR CARRIER ALARM output terminal, to activate an external loss-to-transmit-carrier alarm. The loss-of-transmit-carrier alarm can be deactivated by applying a high-level input (+ 6 volts) through OR gate GOA-2, which applies a steady positive level to the 1AM1 Detector and keeps 2-second delay Q9-Q11 deactivated. The positive input to OR gate GOA-2 may be applied from ALARM switch 1A1S6 (DISABLE position(or from bistable FFF-1 ion the talk request generator module when order-wire circuit operation is activated (para 5-23).

d. No-Transition Receive Alarm. The no-transition receive alarm is activated when no data transitions are being applied to the receive output terminals.

(1) Normally, with no alarm condition, signal transitions are applied through AND gate GAI-3 and through AND gates GAS-3 and GAS4 so that each signal transition is applied as a positive pulse to the delay driver. As long as positive pulses are applied to the delay driver (time between transitions is not greater than 200 milliseconds), the delay driver remains inactive, providing a negative output to maintain 5-second delay Q6 through Q11 deactivated. The resultant negative output form 5-second delay Q6 through Q11 is applied to inhibit OR gate GOB-1, in the input interface and common alarm module, keeping ALARM indicator lamp 1A1DS2 in the off condition (*b* (1) above).

(2) If data transitions occur at intervals greater than 200 milliseconds but less than 5 seconds apart, the delay driver provides a positive input to activate the 5-second delay (after 200 milliseconds). The next transition resets the delay driver; consequently, the 5second delay is reset, producing no change in the output.

(3) If no transition is produced after 5 seconds, 5-second delay Q6, QII times out and provides a high-level output (ground) that enables OR gate GOB-1 (input interface and common alarm module), lighting ALARM indicator lamp 1A1DS2 (*b*(3 above). The ground output from 5-second delay Q6, Q11 turns on amplifier IN-13, providing a ground output that is applied to the NO TRANSITION ALARM REC output terminal, to activate an external no-transition receive alarm.

(4) The no-transition receive alarm may be deactivated by applying a high level (+ 6 volts) through OR gate GOA-3 to the delay driver, keeping the delay driver deactivated, and holding ALARM indicator lamp 1A1DS2 off ((1 above. The high-level input may be applied from ALARM switch lAlS6 (DISABLE position l or from bistable FFB-1 (talk-request detection module) when a talk-request signal has been detected, signifying the order-wire circuit mode of operation (para 5-23).

e. Loss-of-Receive-Carrier Alarm. This alarm is activated when the input fsk signals applied to the receive input terminals are interrupted or fall below a predetermined level, for 2 seconds or longer.

(1) With input fsk signals applied, the output of third input amplifier Q15 is applied through REC CARRIER ALARM THRESHOLD resistor 1A1R11 to the level threshold, which provides a polar signal (+ 6 volts) to amplitude detector Q7, Q8, Q9. The amplitude detector provides a low-level output that is inverted by amplifier IN-10, providing a high-level output (+ 6 volts) through amplifier IN-9. Amplifier IN-9 provides a low-level output to activate 2-second delay Q11, Q12 (adjustable by REC CARRIER ALARM TIME control resistor 1A1R12), producing a low level for OR gate GOB-1 (input interface and common alarm module) that holds ALARM indicator lamp 1A1DS2 in the off condition (*b* (1) above).

(2) When the receive carrier is lost, the amplitude detector provides a high-level output equivalent to no output from the detectors to amplifier IN-10. The resultant, inverted, low-level output provides a low-level input to amplifier IN-9. The high-level output from amplifier IN-9 activates 2-second delay Q11, Q12.

(a) If the input receive carrier is restored within a 2-second interval, the amplitude detector provides a low level to amplifier IN-10, turning off ALARM indicator lamp 1A1DS2 as described in (1) above.

(b) If the input carrier is lost for more than 2 seconds, 2-second delay Q11, Q12 times out, providing a high level (+ 6 volts) to OR gate GOB-1 in the input interface and carrier alarm module and causing ALARM indicator lamp 1A1DS2 to be lighted (*b*(2)

above). The high-level output of 2second delay Q11, Q12 is also inverted by amplifier IN-11 and applied as a ground to LOSS OF REC CARRIER ALARM output terminals to activate an external loss-of-receive-carrier alarm.

(3) The loss-of-receive-carrier alarm may be deactivated by applying a high level (+ 6 volts) through OR gate GOC-1 to amplifier IN-9, which keeps 2-second delay Q11, Q12 deactivated ((1) above) and holds ALARM indicator lamp 1AlDS2 in the off condition. The positive input may be applied from ALARM switch 1A1S6 (DISABLE position) or from bistable FFB-1 (talk-request detection module), when a talk-request signal has been detected, signifying the order-wire circuit mode of operation (par 5-23).

f. Common Alarm Circuitry.

(1) The common alarm circuitry in the input interface and common alarm module includes OR gate GOB-1 and amplifiers IN-5 and IN-6. A high-level input (+ 6 volts) applied from any of the four alarm circuits (*b* through *e* above) enables GOB-1, providing a high-level output that is inverted by amplifier IN-5 and applied as a low level to light ALARM lamp 1A1DS2.

(2) By strapping terminals 2 and 3 together, the common alarm enable level is inverted by amplifier IN-6 and applied as a low level (ground) to the SYNCHRONIZER DISABLE OUT output terminal, for use as a common alarm. If straps 1 and 2 are connected together, the + 6 volts output from amplifier IN-10 in the receive input and carrier alarm module (+ 6 volts output immediately upon loss of input carrier) is inverted by amplifier IN-6 and applied as a low level (ground) to the SYNCHRONIZER DISABLE OUT output terminal, to disable any external synchronizing equipment that requires output from the MD-674(P)/G to maintain synchronism.

CHAPTER 6
DIRECT SUPPORT AND GENERAL SUPPORT AND DEPOT MAINTENANCE

6-1. General

a. Troubleshooting at direct support, general support, and depot maintenance categories includes all techniques outlined for organizational maintenance and any special or additional techniques required to isolate a defective part. These maintenance procedures supplement the procedures described for organizational maintenance. The systematic troubleshooting procedures, which begins with the operational and sectionalization checks performed at an organizational category must be completed by further localizing and isolating techniques. Refer to appendix C to determine the maintenance function allocated to each category of maintenance and the tools and test equipment authorized to perform the maintenance function.

b. Troubleshooting may be performed while the equipment is operating as part of a system, or after it has been removed from service. When troubleshooting is performed while the equipment is operating as part of a system, it is normally done by organizational personnel. When troubleshooting is done with the equipment removed from service, perform the operational tests (para 6-3) to determine symptoms to aid in locating the trouble.

6-2. Troubleshooting Procedures

a. Sectionalization. Sectionalization procedures normally performed at an organizational category (ch 4) sectionalize the trouble to a defective MD-674(P)/G or printed-circuit card. When a defective MD-674(P)/G or printed-circuit card is received, localize the trouble to a stage (*b* below) and then isolate the trouble within the stage (*c* below).

b. Localization. Perform the operational test (para 6-3) with the defective MD-674(P)/G or defective printed-circuit card installed in the MD-674(P)/G available for maintenance. If the correct results are not obtained during the operational tests, refer to the troubleshooting chart (para 6-4) to localize the trouble to a stage. Then isolate the trouble within the stage (*c* below).

c. Isolation. When the trouble has been isolated to a stage (*b* above), isolate the trouble to the defective part by using the procedures described in paragraph 6-5.

d. Deleted.

6-3. Operational Tests

a. Test Equipment Required. See Maintenance Allocation Chart Section III for test equipment.

b. Preliminary Procedures.

(1) Slide the modem chassis of the test MD-674(P)/G out of the ferrous case (para 2-4).

(2) If an entire MD-674(P)/G is to be repaired, disconnect the connecting cable from the rear of the test MD-674(P)/G (fig. 1-4), depress the slide release buttons on the slide assembly, and remove the modem chassis of the test MD-674(P)/G from the case. Install the chassis of the defective MD-674(P)/G in the ferrous case, and connect the cable to the rear connector. Make sure that all plug-in assemblies are installed.

(3) If a PC card assembly or other plug-in assemblies is to be tested, remove its counterpart from the test MD-674(P)/G and install the defective assembly in its place.

(4) Connect the MD-674(P)/G for loopback operation (fig. 6-1).

(5) Operate the controls of the various equipments as indicated in the chart below.

Equipment	Control	Position
Power Supply PP-205A (p/o Stelma DAC-6A).	POWER	Off.
	INTENSITY	ON.
	MARKERS.	
	INTERNAL SWEEP MILLISECONDS COURSE.	75-300.
	INTERNAL SWEEP MILLISECONDS FINE.	Counterclock-wise.
	SWEEP OPTIONS.	AUTO.
Data Scan Scope DSS-205A (p/o Stelma DAC-6A).	POWER.	OFF.
	CHARACTER BLANKING.	OFF.
	VERTICAL GAIN and CENT.	Midposition.
	INTENSITY	Counterclock-wise
	FOCUS and ASTIGMATISM.	Midposition.
	HORIZONTAL GAIN and CENT.	Midposition.
	INPUT POLARITY.	----
	INPUT SELECT ..	LOW LEVEL.
	INPUT FILTER....	IN.
Distoration Analyzer DD-205A (p/o Stelma DAC-6A).	BAUDS	Determined by low speed modem.
	SYNCHRONOUS-START-STOP.	SYNCHRO-NOUS.
	UNIT INTERVALS.	10.
	TRANSITION SELECT:	
	Left hand.....	MARK
	Right hand.....	SPACE.
Pattern Generator PG-205A (p/o Stelma DAC-6A).	DISTORTION SELECT.	ALL.
		AVG.
	RESET.....	
	DISTORTION.....	AUTO.
	TENS PERCENT DISTORTION.	OFF.
		0.
	UNITS PERCENT DISTORTION.	
	SYNCHRONOUS-START-STOP.	SYNCHRONOUS.
	MARK-SPACE 1 through 8.	SPACE.
	LEVEL CODE.....	8.
	BAUDS.....	Determined by MX-73(*)/G.
	PATTERN SELECTOR.	REVERSALS
	CHARACTER RELEASE.	FREE RUN.
	JACK SIGNAL SELECTOR.	LOW LEVEL.
MD-674(P)/G	BAUD RATE.....	Determined by MS-73(*)/G.
	INPUT SELECT..	DATA.
	ALARM.....	DISABLE.
	INPUT	50K Ω
	OUTPUT.....	50K Ω

c. Tests.

Note.

Be sure all strapping options are connected

(1) Operate the POWER switches on the PP-205A and on the MD-674(P)/G to ON. The SIGNAL indicator lamp on the DD-205A should be lighted, the front panel meter should indicate zero distortion, and the reversals pattern should be observed on the DSS-205A after adjustment of the VERTICAL, INTENSITY, FOCUS, HORIZONTAL, and INTERNAL SWEEP MILLISECONDS controls of the DSS-205A; the ALARM lamp on the MD-674(P/G front panel should be extinguished.

(2) Operate the ALARM switch on the MD-674(P)/G (fig. 2-3) to NORM; the ALARM indicator lamp should remain extinguished, and all other indications should be as indicated in (1) above.

(3) Operate the INPUT SELECT switch (fig. 2-3) to MARK. The ALARM indicator lamp should light, and a zero voltage (ground) should be measured at the

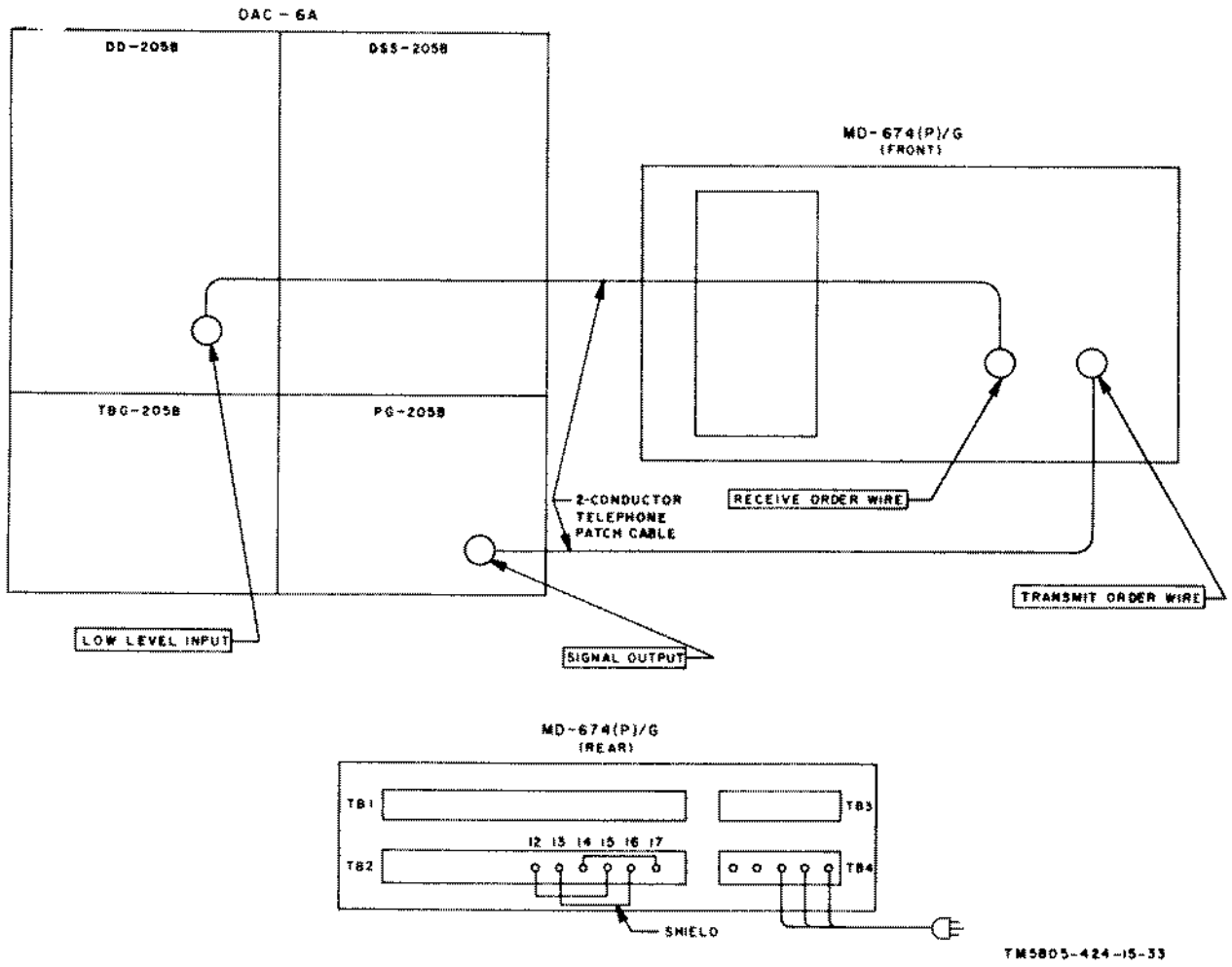


Figure 6-1. Operational tests, connection diagram.

no-transition alarm send terminals and the no-transition alarm receive terminals at the rear of the unit (fig. 2-2). Plus 6 volts should be measured at the loss-of-transmit-carrier alarm terminals and the loss-of-receive-carrier alarm terminals at the rear of the unit.

(4) Operate the INPUT SELECT switch (fig. 2-3) to SPACE; indications should be as in (3) above.

(5) Operate the INPUT SELECT switch to OFF. In addition to the indications in (3) above, a positive 6 volts should be measured at the loss-of-transmit-carrier alarm terminals and at the loss-of receive-carrier alarm terminals at the rear of the unit (fig. 2-2).

(6) Operate the INPUT SELECT switch (fig. 2-3) to DATA, and disconnect one lead from the balanced receive carrier input terminals at the rear of the unit (fig. 2-2). The ALARM indicator lamp should light, and a ground (O volt) should be measured at the no-transition alarm receive terminals and the loss-of-receive carrier alarm terminals at the rear of the unit (fig. 2-2). Plus 6 volts should be measured at the no-transition alarm send terminals and the loss-of-transmit-carrier alarm terminals at the rear of the unit. The DSS-205A should indicate a steady mark.

(7) Reconnect the lead to the balanced receive carrier input terminals. The ALARM in-

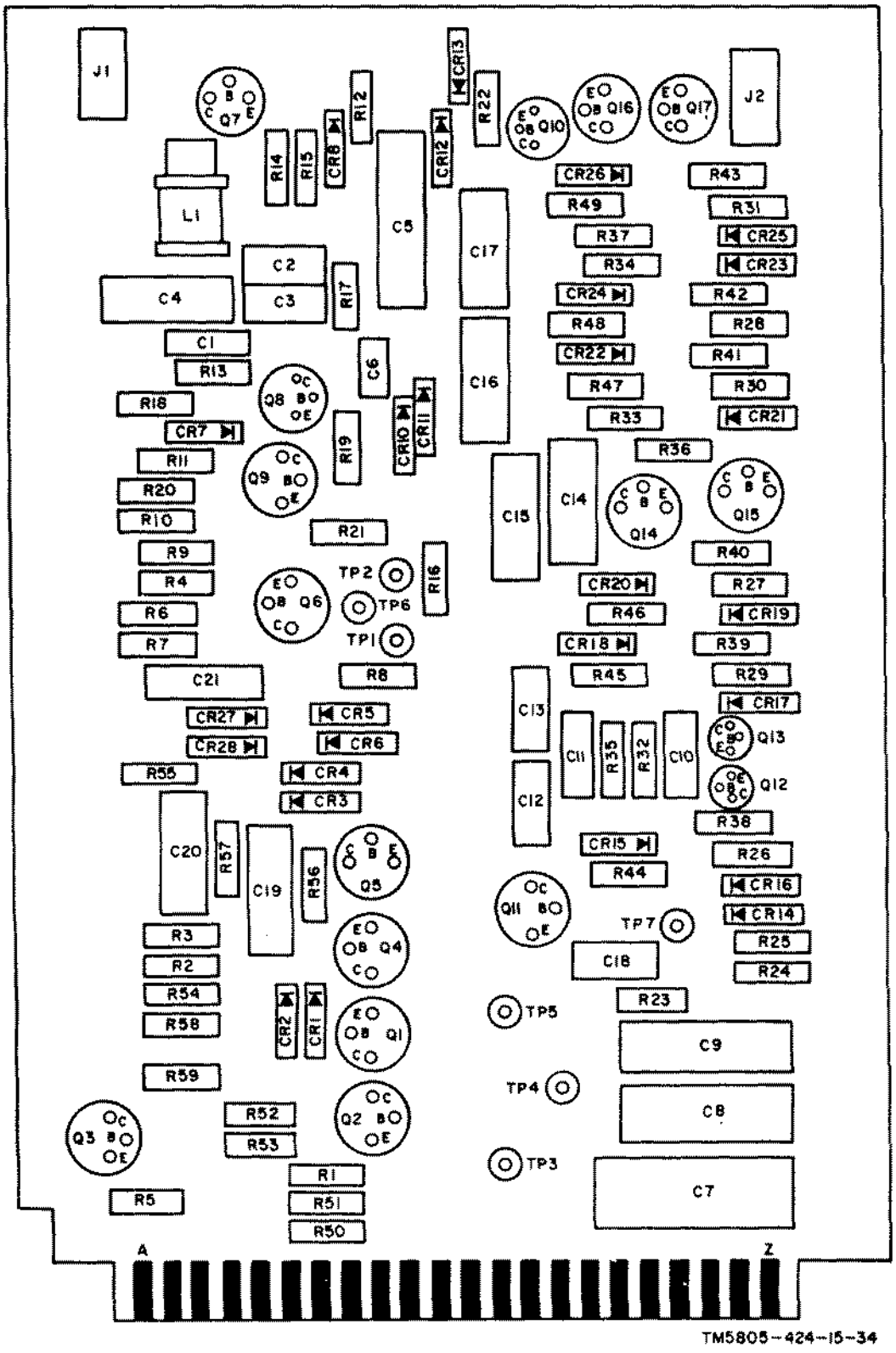


Figure 6-2. Printed-circuit cord assembly A1 (PC 80034090), component location diagram.

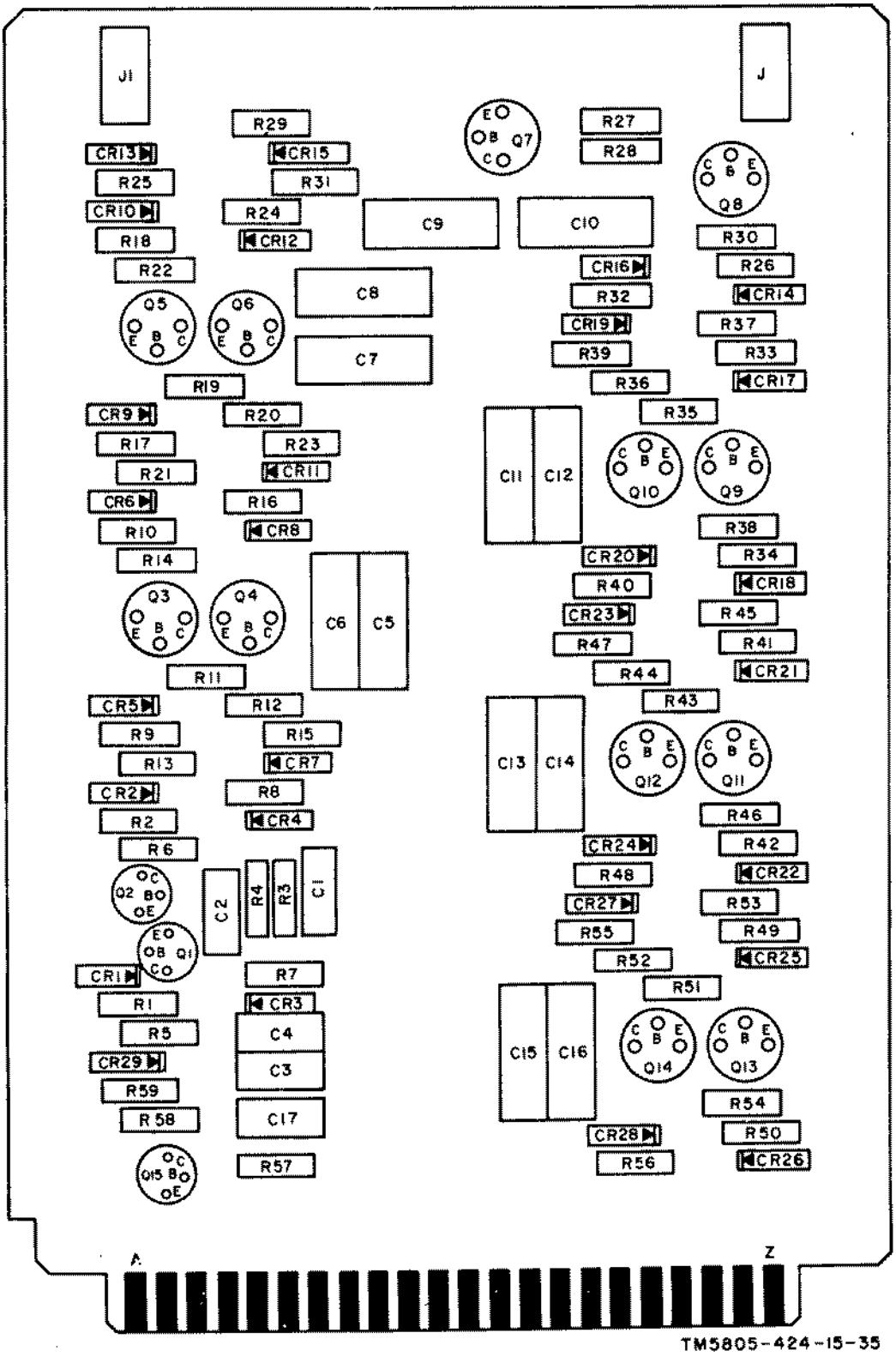


Figure 6-3. Printed-circuit card assembly A2 (PC 80034100),component location diagram.

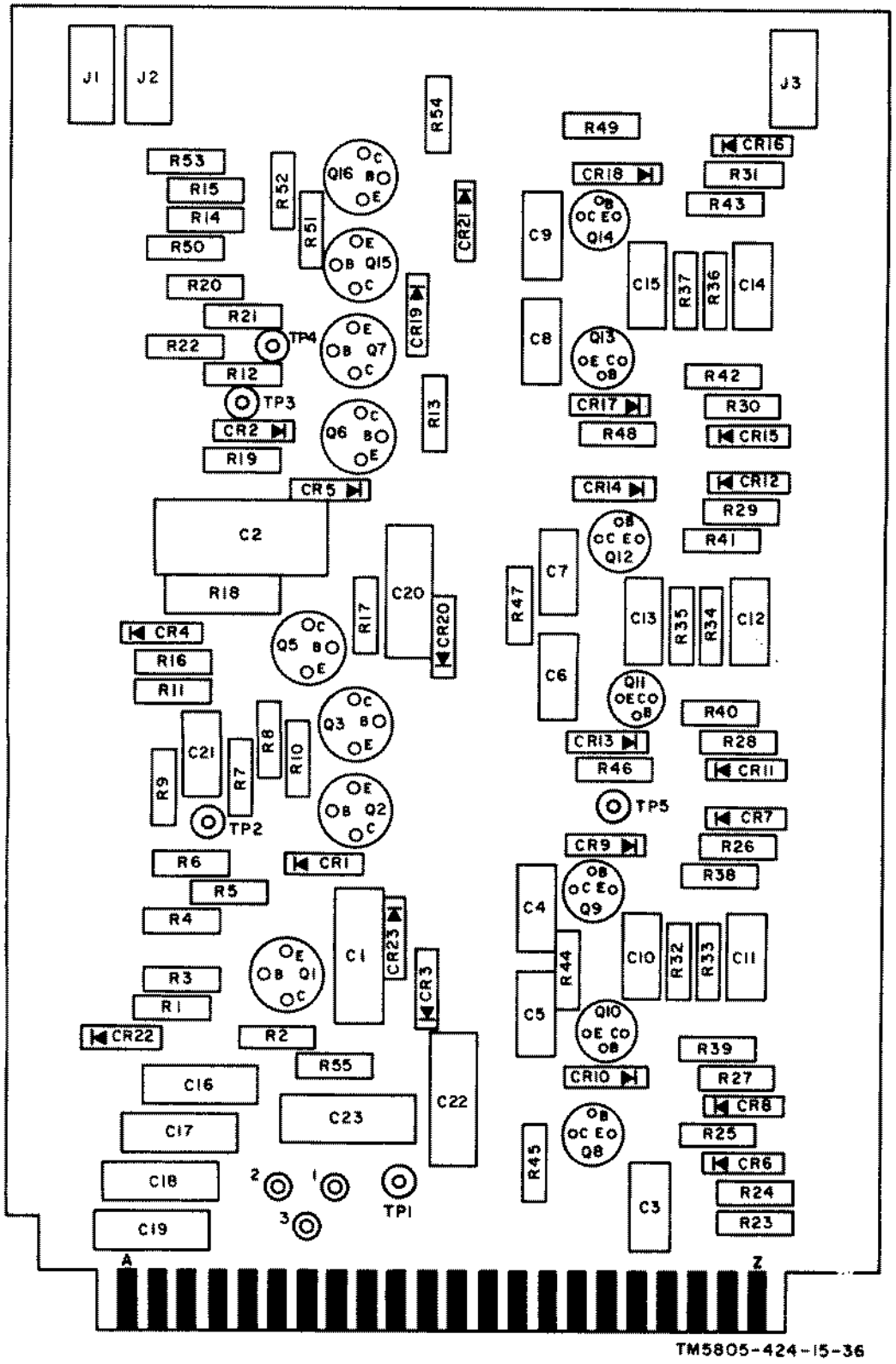


Figure 6-4. Printed-circuit card assembly A3 (PC 80034140), component location diagram.

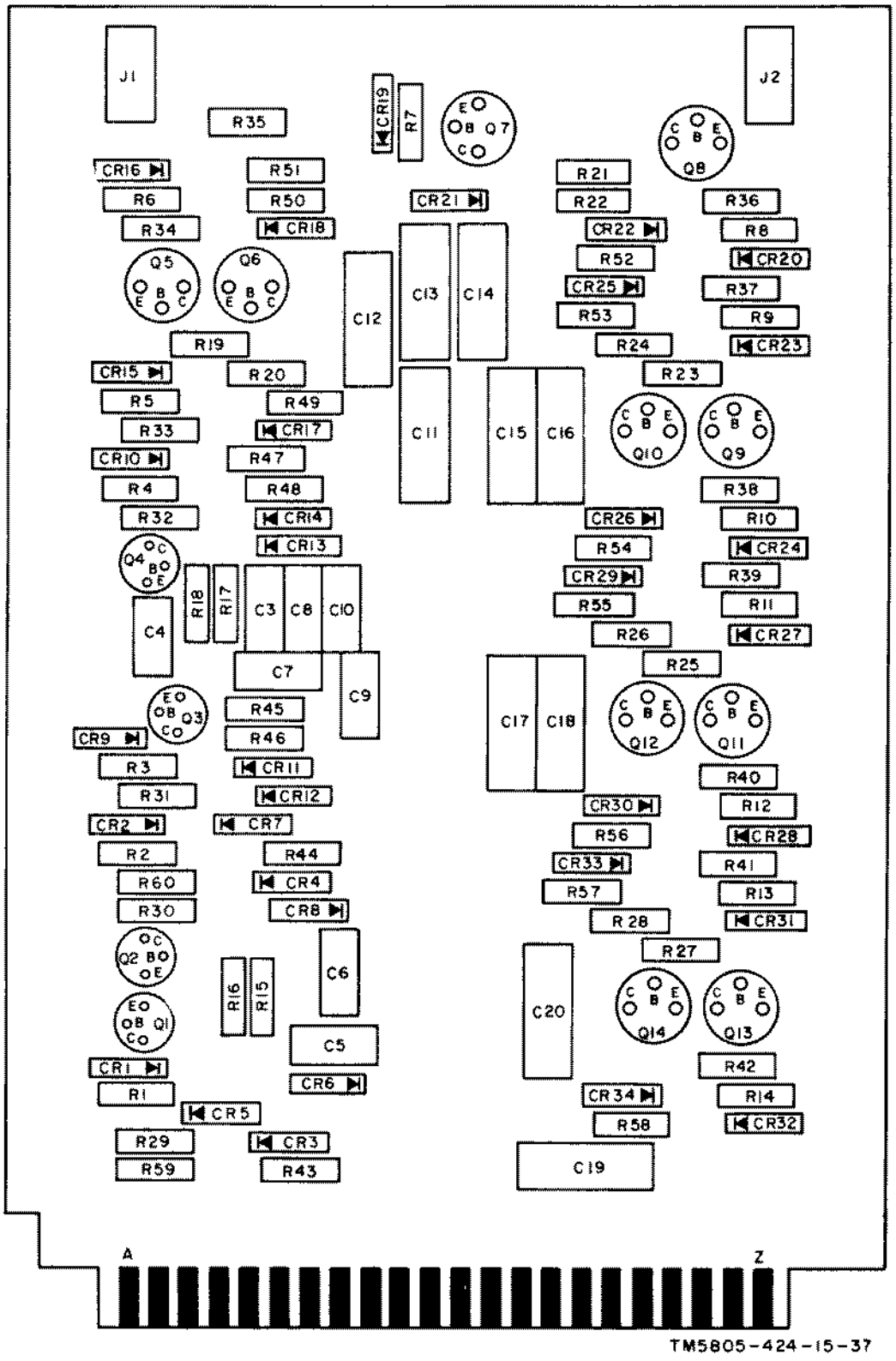


Figure 6-5. Printed-circuit card assembly A4 (PC 80034080), component location diagram.

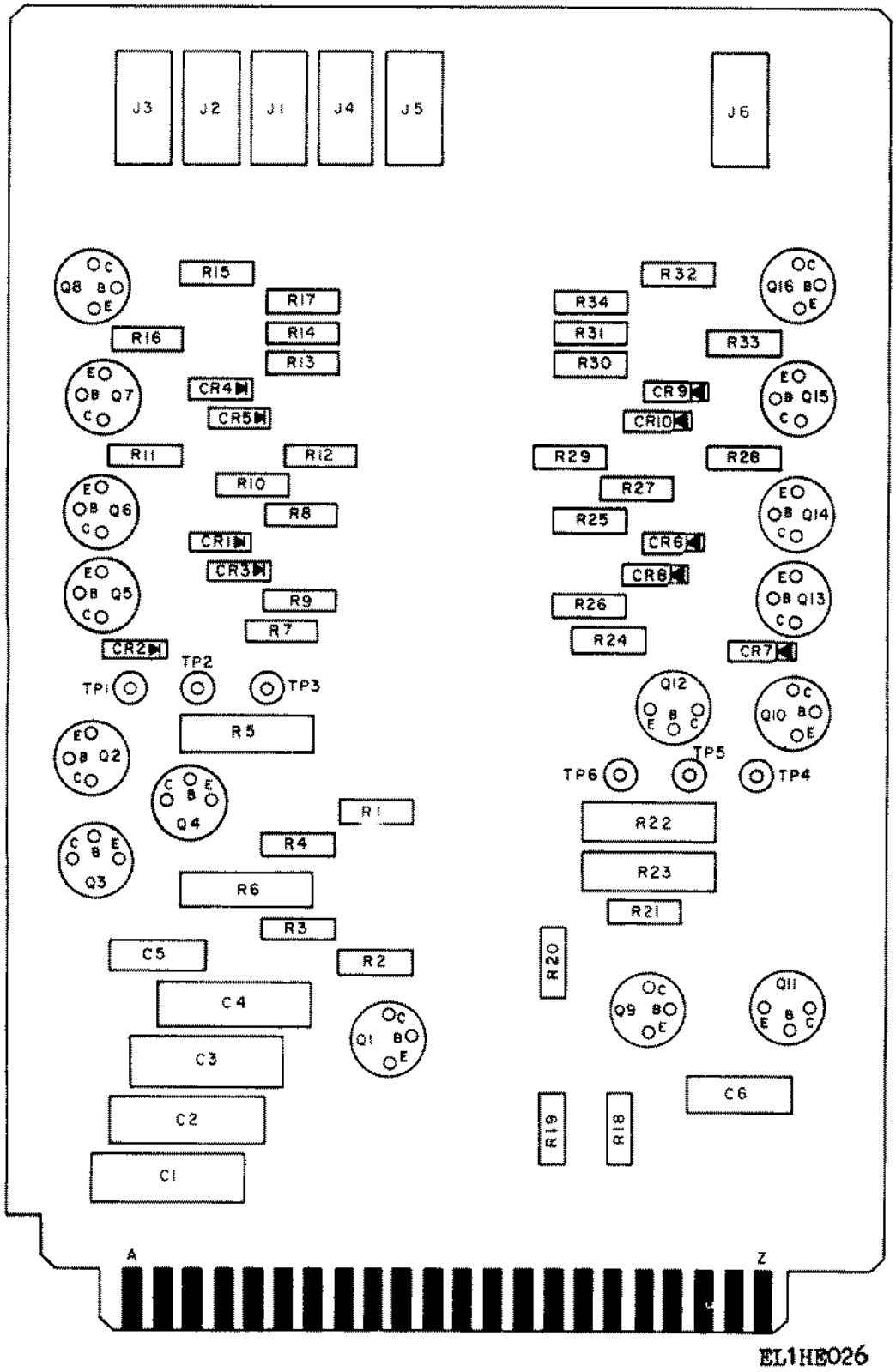


Figure 6-6. Printed-circuit card assembly A5 (PC 80034150), component location diagram.

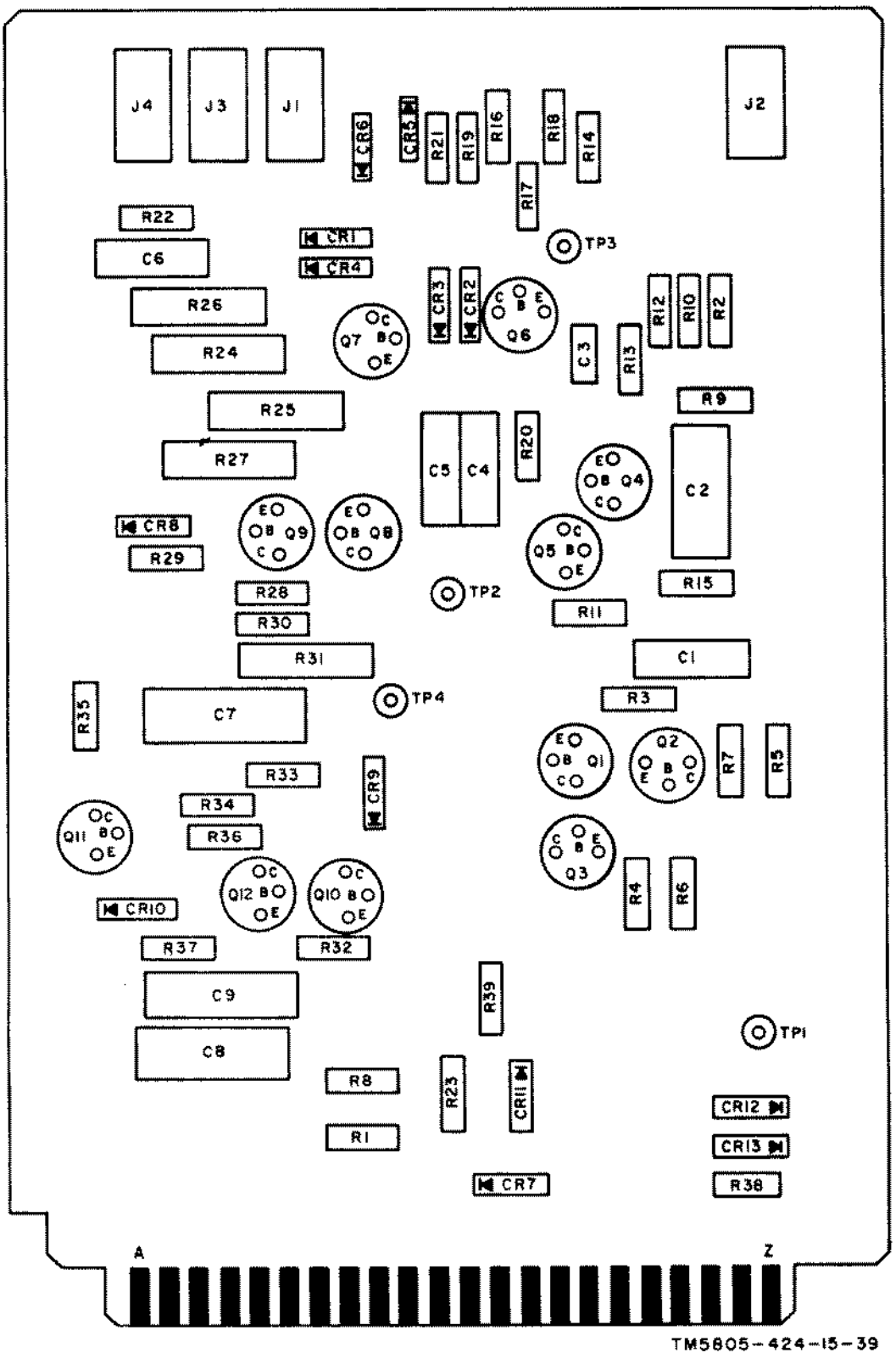


Figure 6-7. Printed-circuit card assembly A6 (PC 80034120), component location diagram.

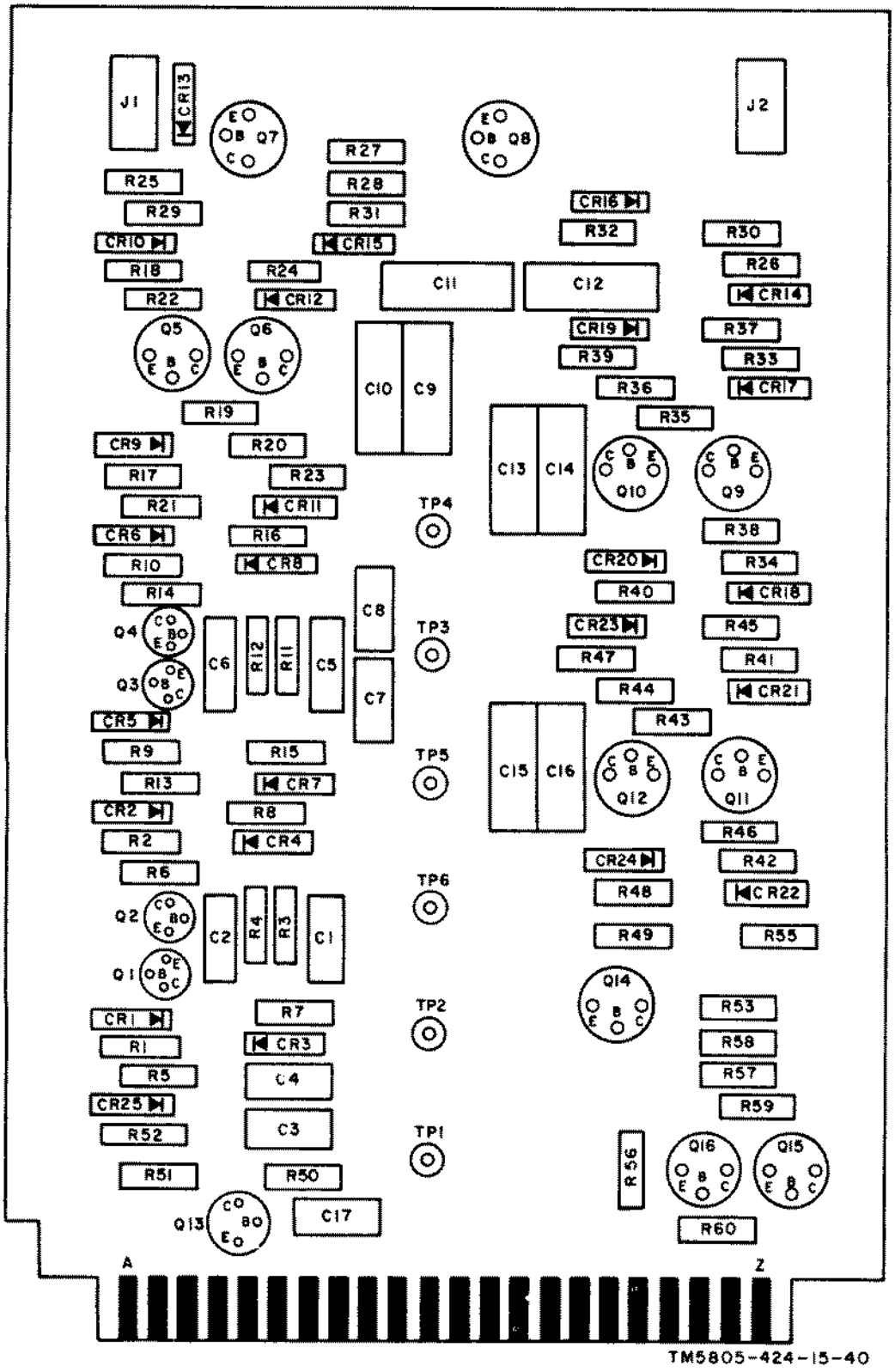


Figure 6-8. Printed-circuit card assembly A7 (PC 80034130), component location diagram.

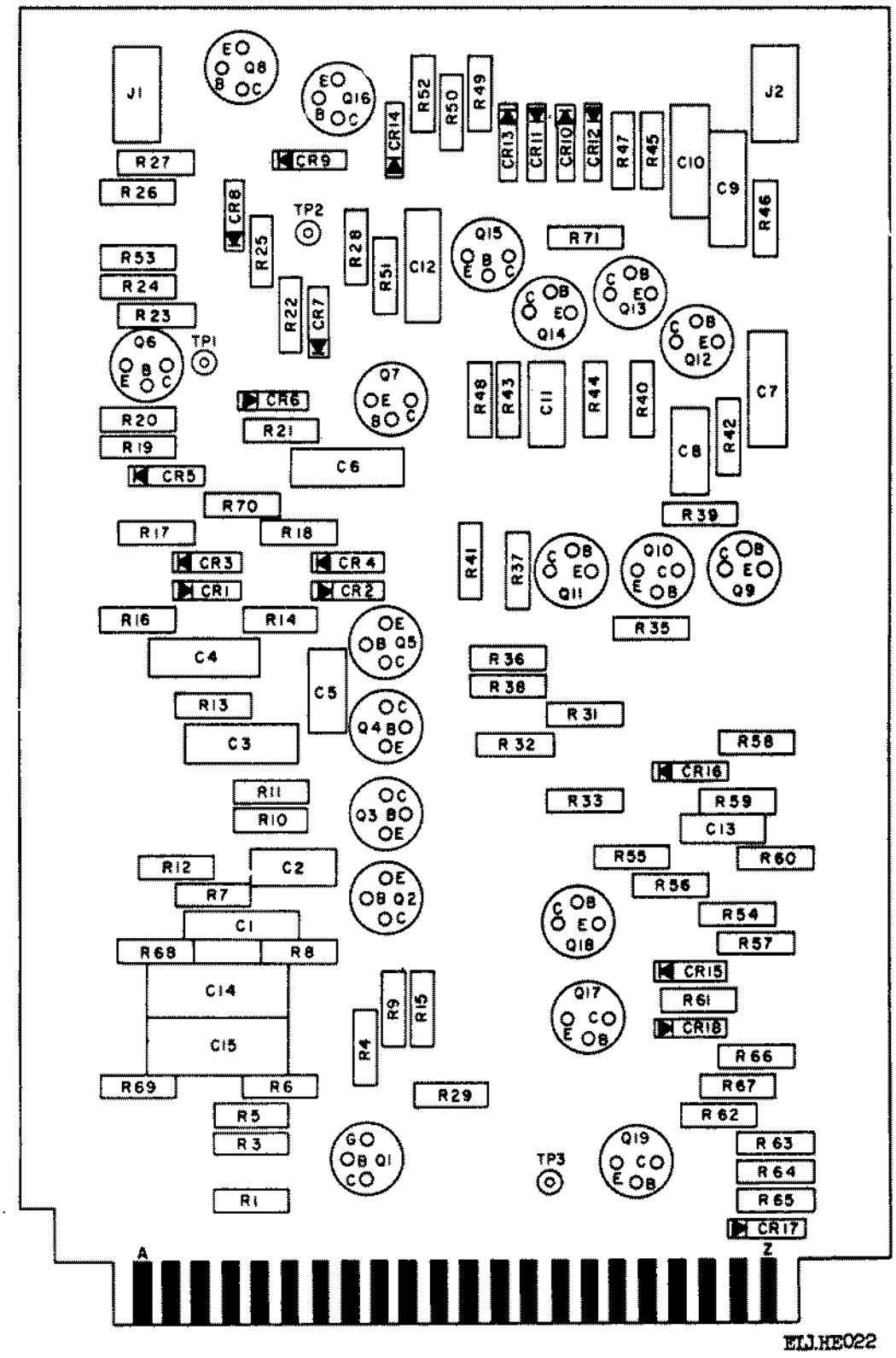


Figure 6-9. Printed-circuit card assembly A8 (PC 80034020), component location diagram.

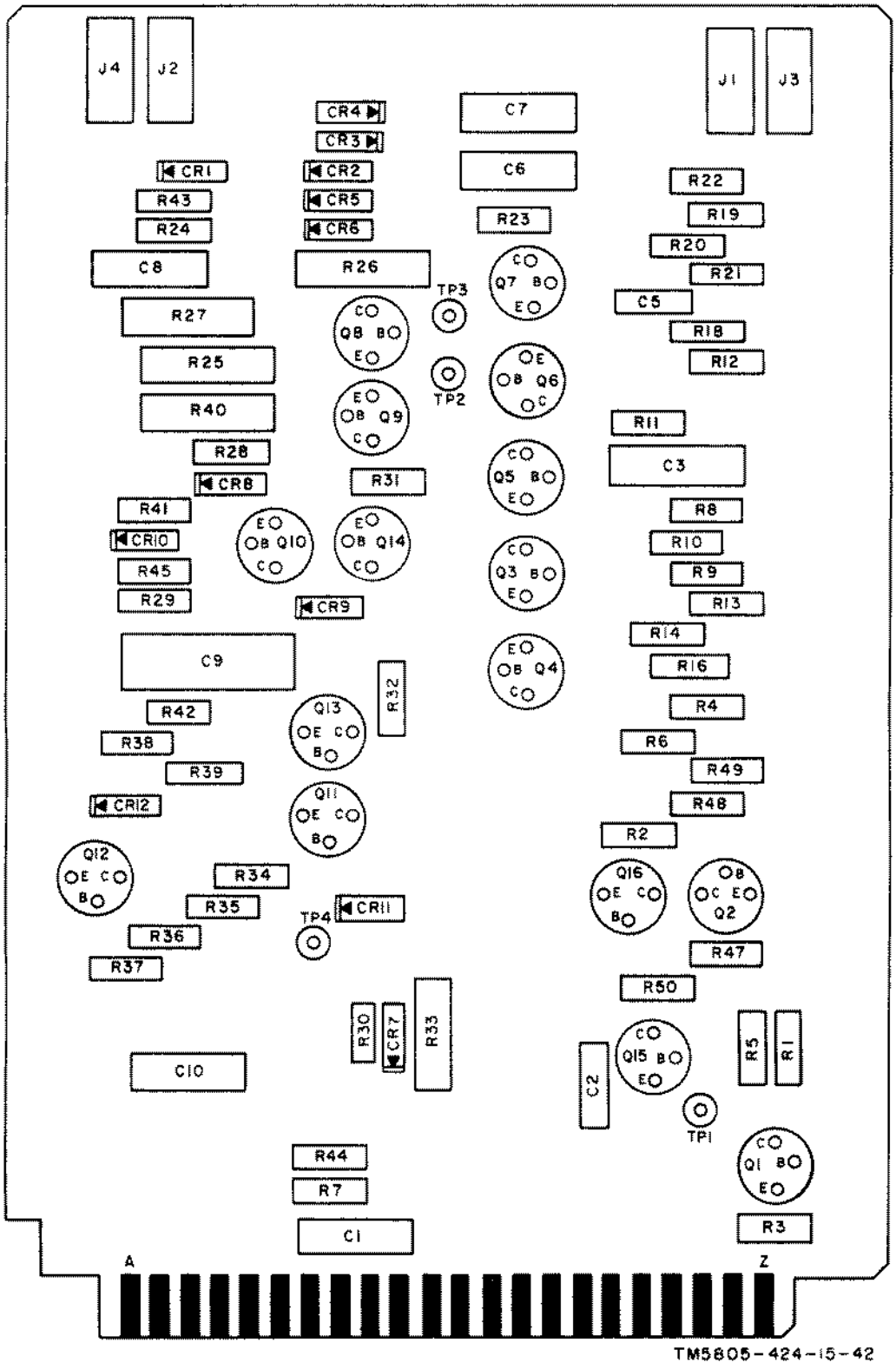


Figure 6-10. Printed-circuit card assembly A9 (PC 80034050), component location diagram.

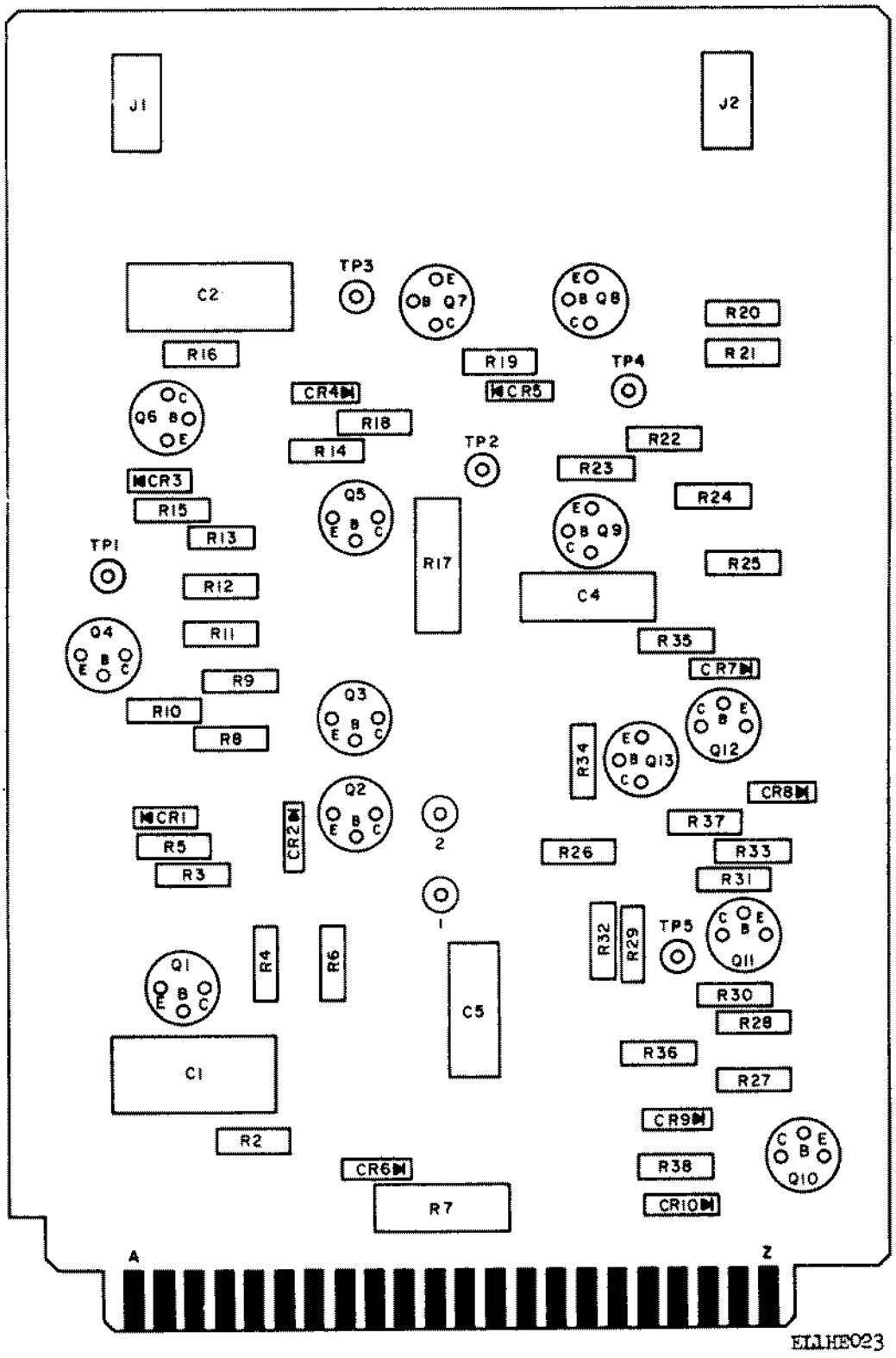


Figure 6-11. Printed-circuit card assembly A10 (PC 80034040), component location diagram.

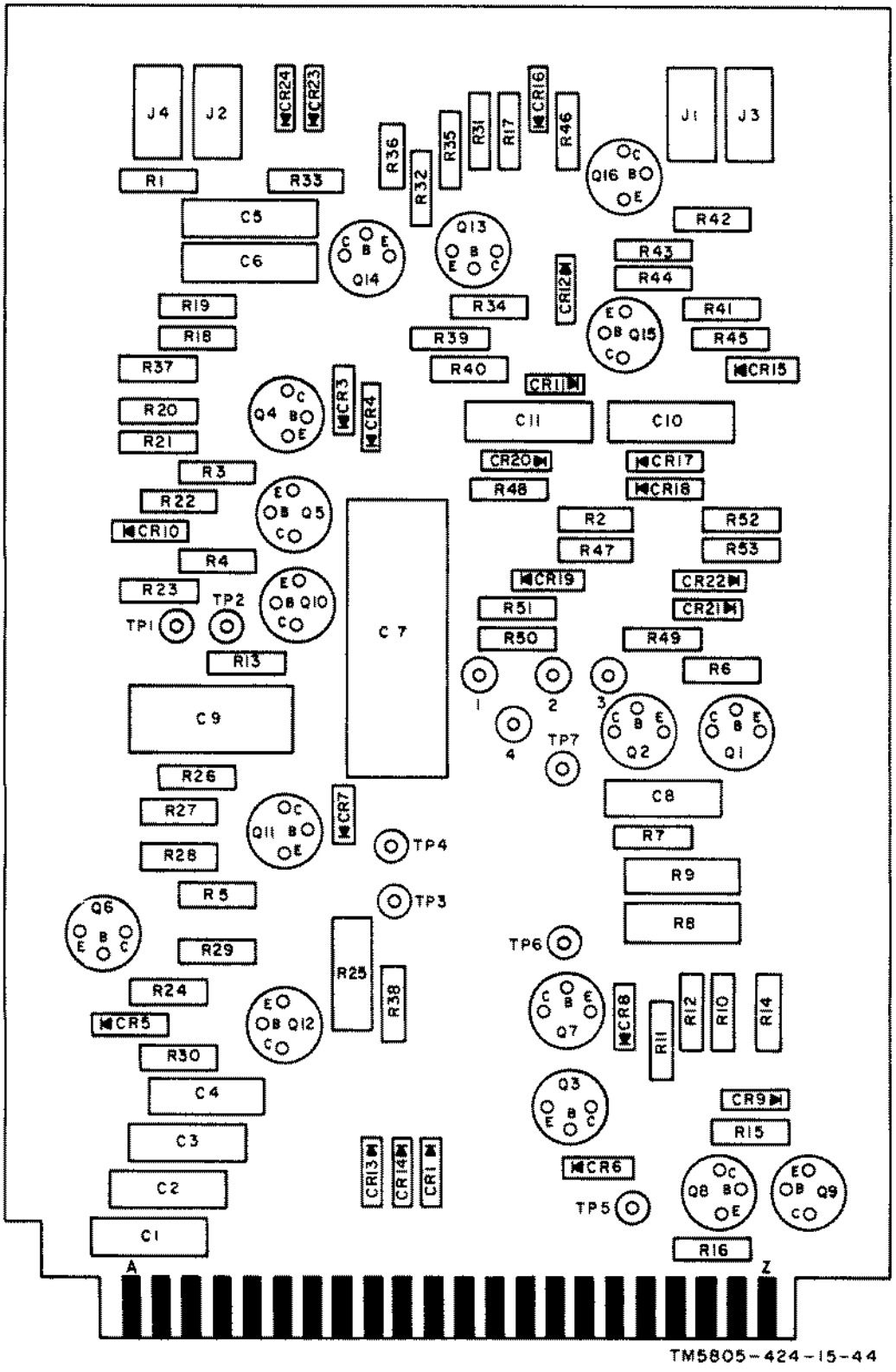


Figure 6-12. Printed-circuit card assembly A11 (PC 80034030), component location diagram.

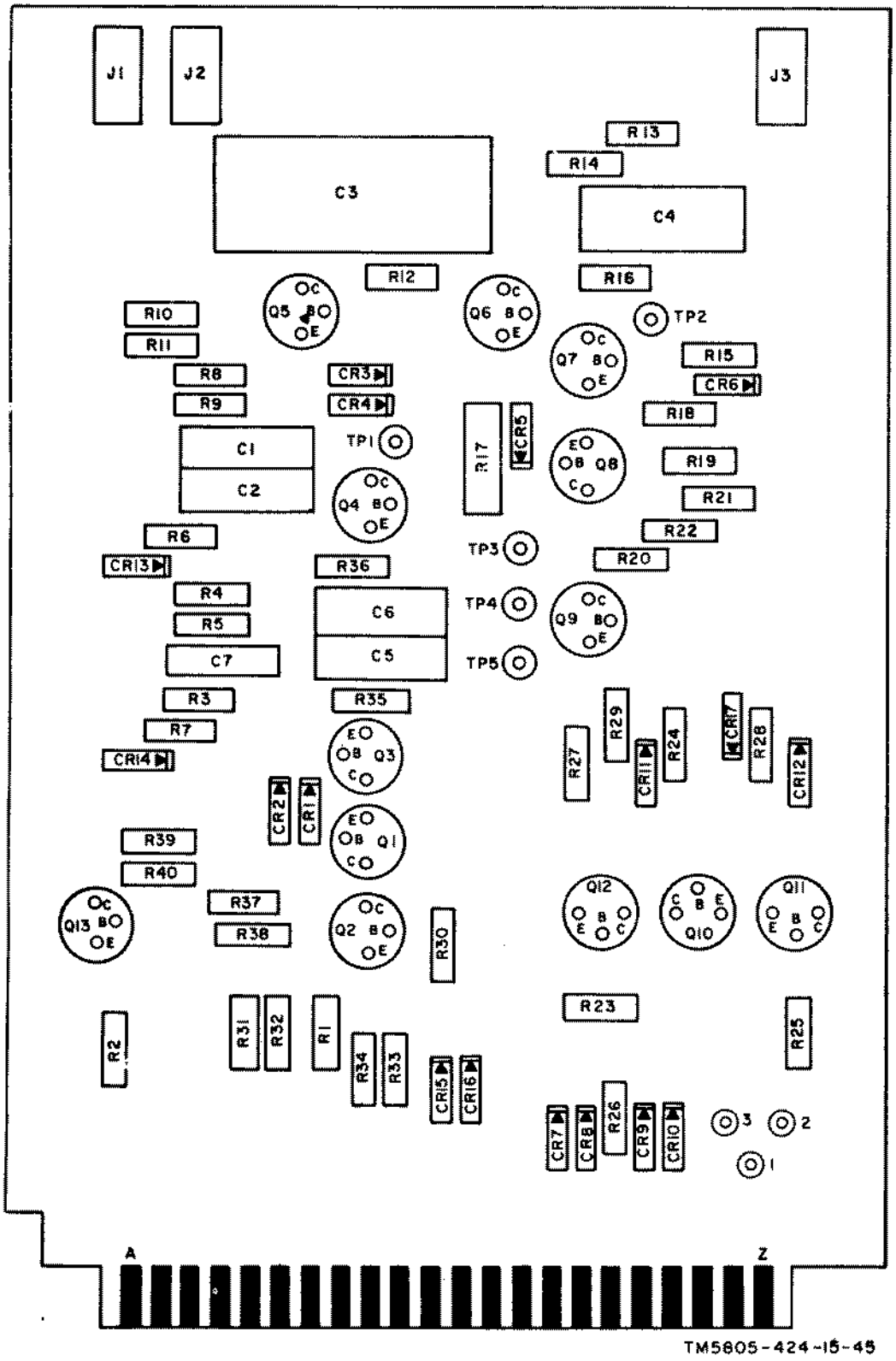


Figure 6-13. Printed-circuit card assembly A12 (PC 80034060), component location diagram.

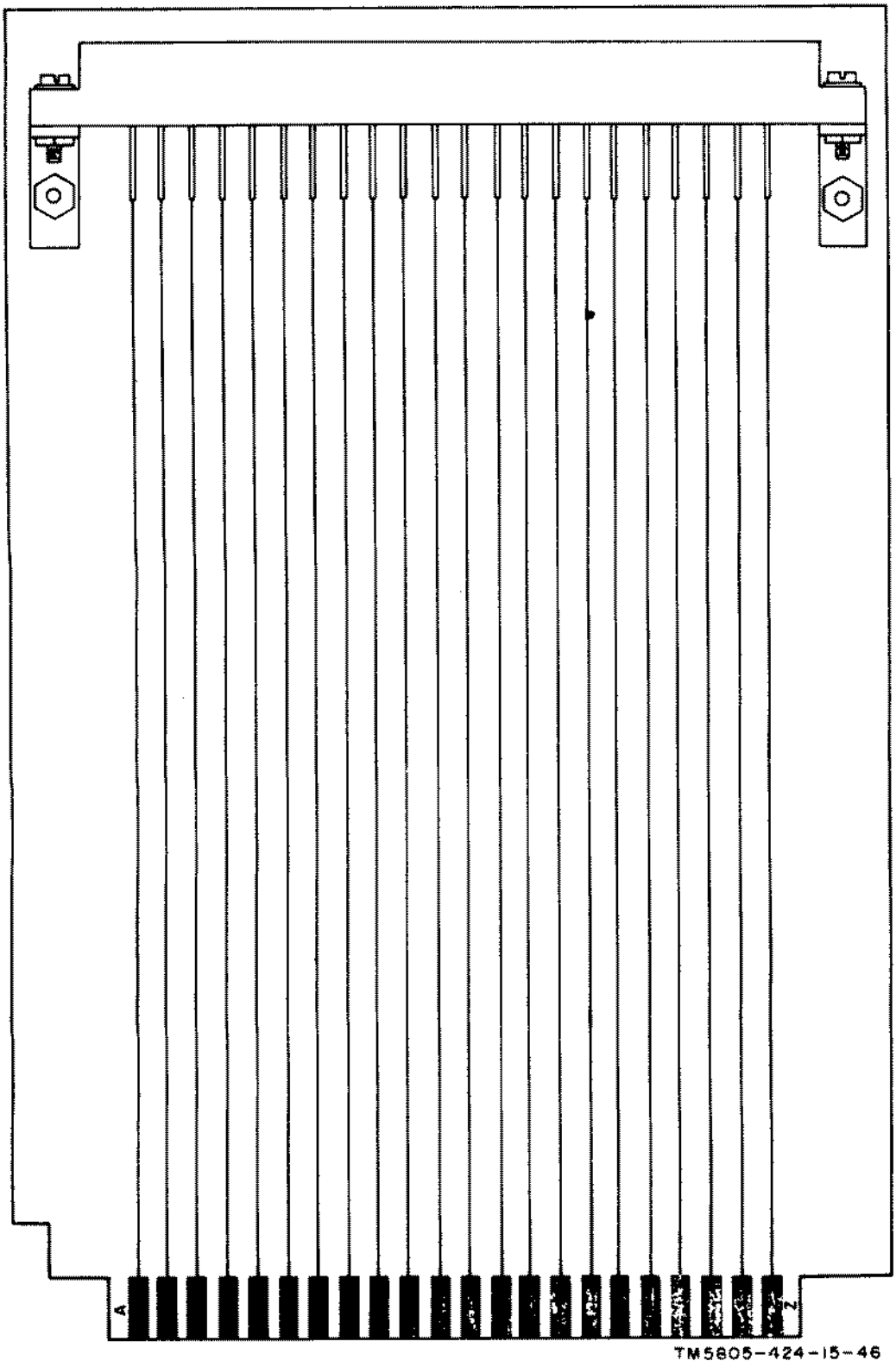


Figure 6-14. Printed-circuit card assembly A13 (PC 80034010), adapter card diagram.

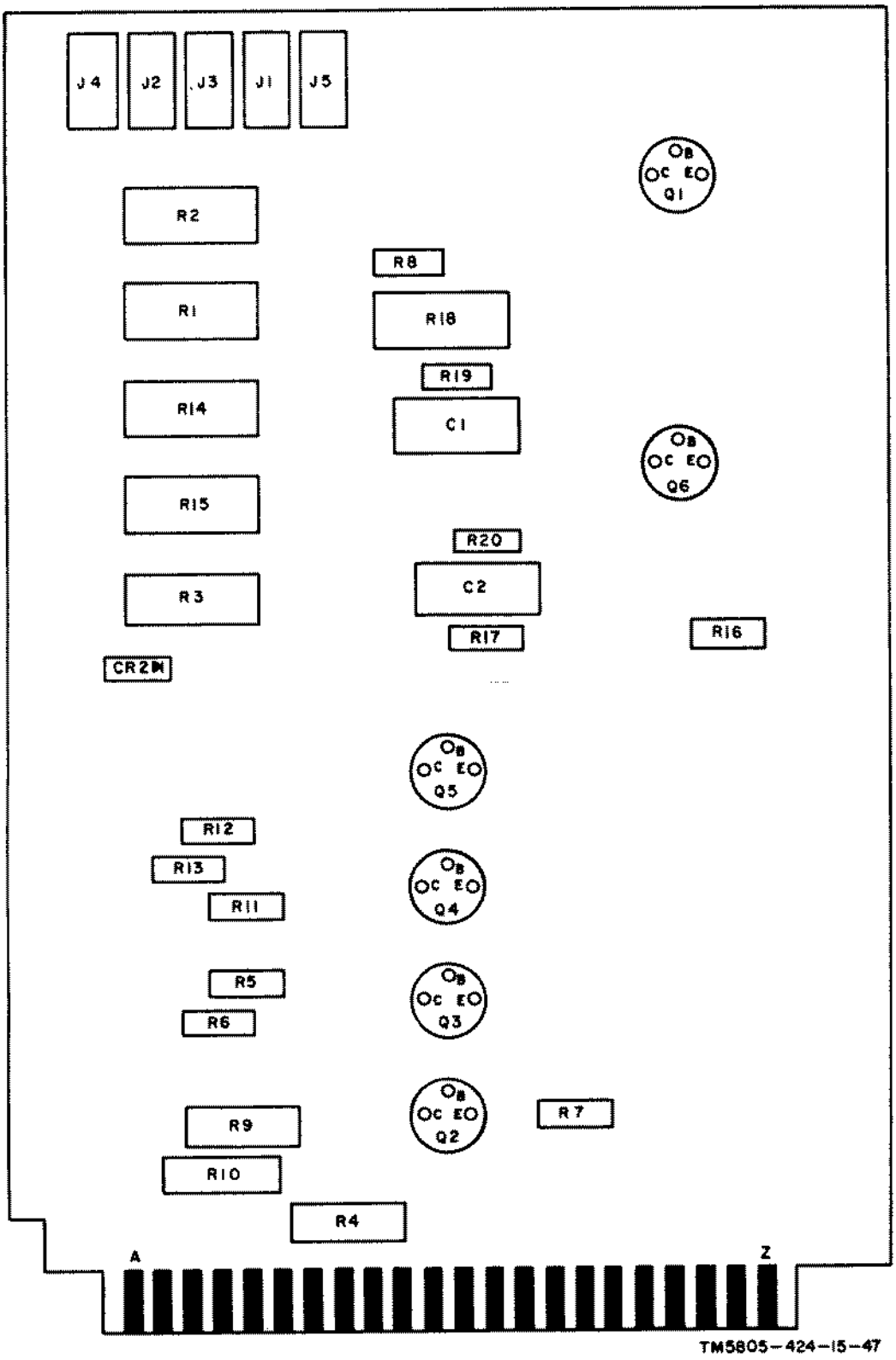


Figure 6-15. Printed-circuit card assembly A14 (PC 80034170), component location diagram.

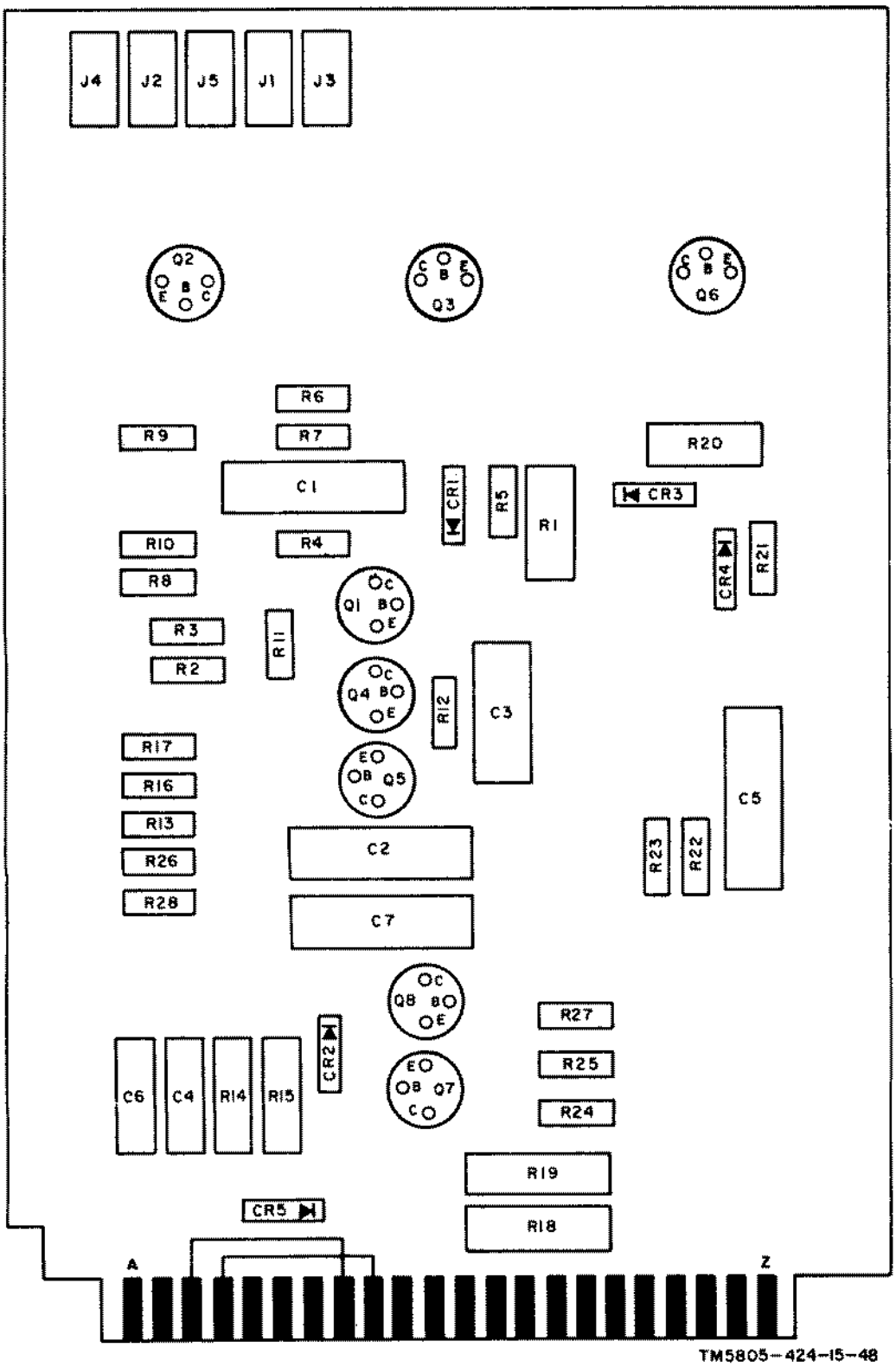


Figure 6-16. Printed-circuit cord assembly A15 (PC 80034160), component location diagram.

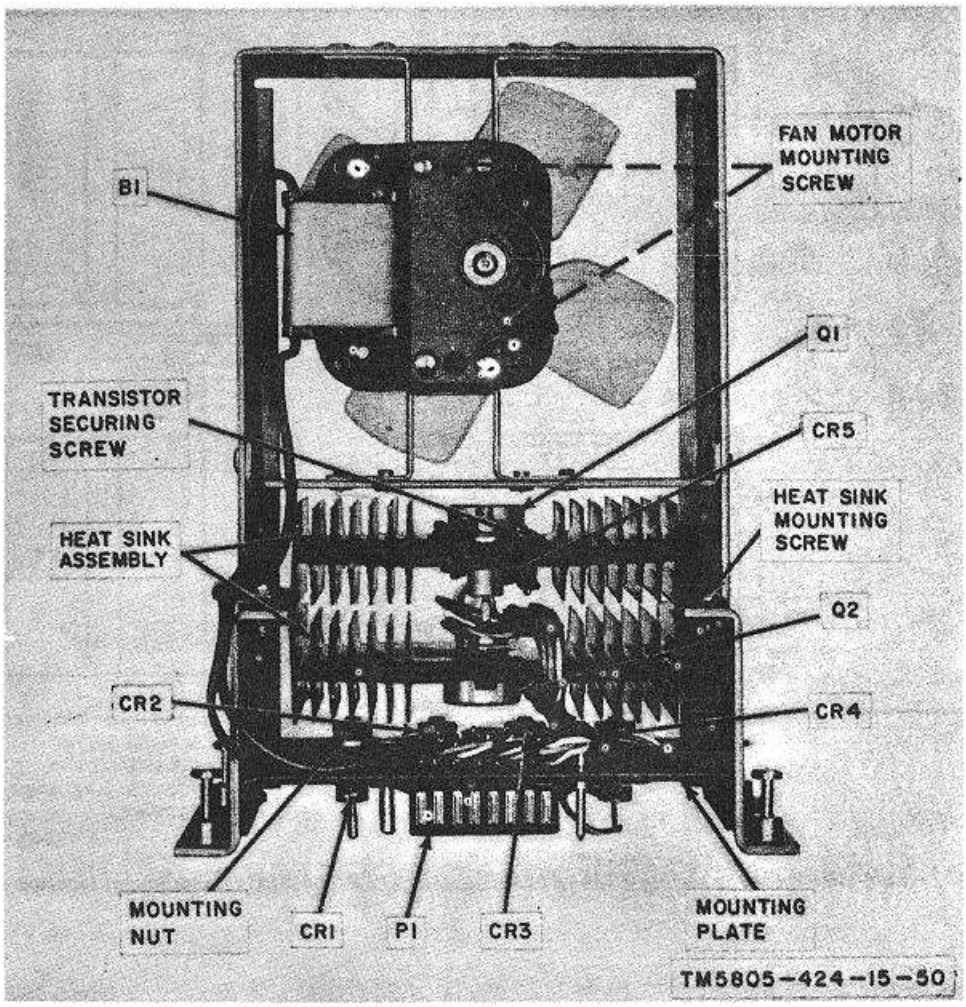


Figure 6-18. Power supply submodule, component location diagram.

dicator lamp should be extinguished, and the reversals test pattern should be observed on the DSS-205A.

(8) Remove the patch plug from the ORDER WIRE SEND test jack on the front panel. The ALARM indicator lamp should be lighted, and the DSS-205A should indicate a steady mark.

(9) Depress the TALK REQUEST pushbutton on the MD-674 (P)/G front panel. The ALARM indicator lamp should be extinguished, and then the TALK REQUEST indicator lamp should be lighted.

(10) Depress the TALK REQUEST RESET pushbutton. The ALARM indicator lamp should be lighted and the TALK REQUEST indicator lamp should be extinguished.

(11) Check for bit-timing signals at the four timing output terminals at the rear of the MD-674(P)/G (fig. 2-2) with an oscilloscope. Bit-'timing signals should be present at all four terminals at all times during the operational tests described above.

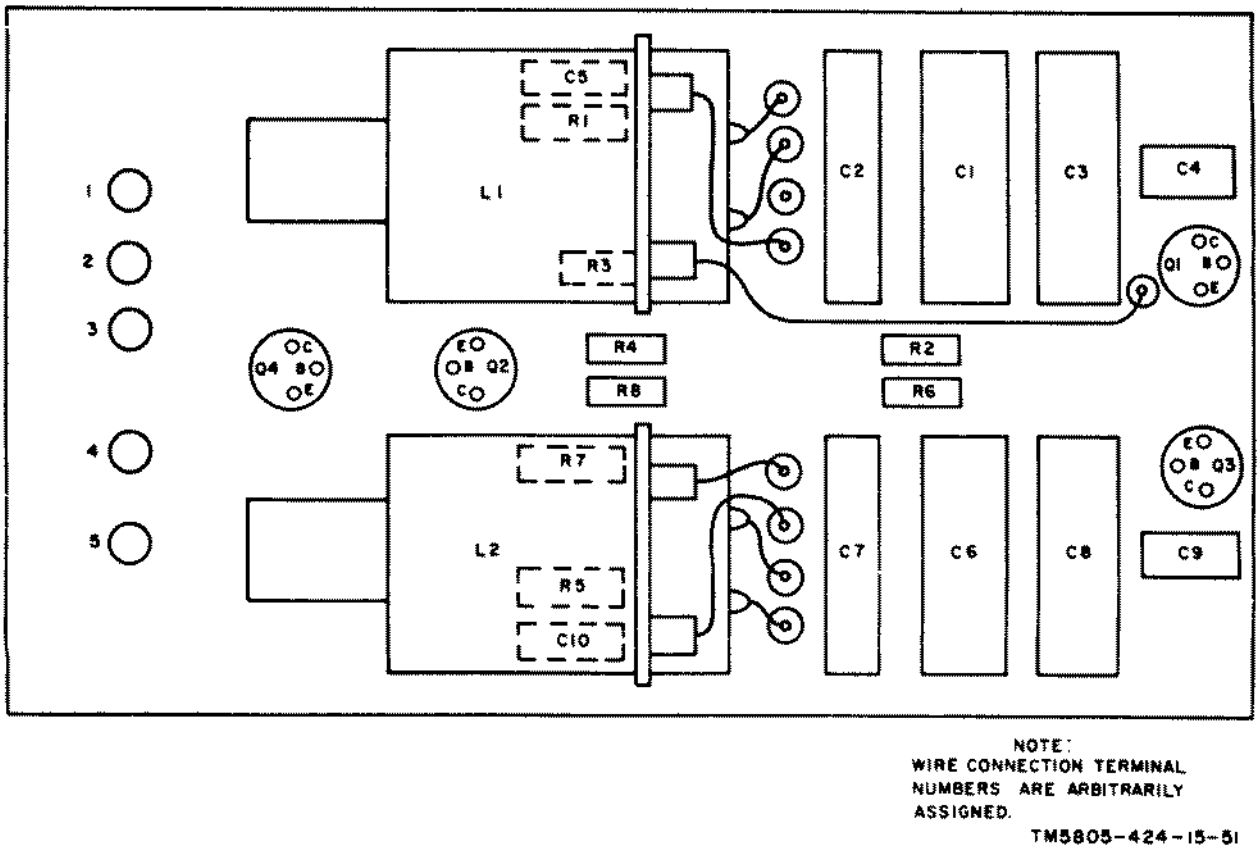


Figure 6-19. Printed-circuit card assembly A18A1A1 through AS1A1 (PC 80034210), component location diagram.

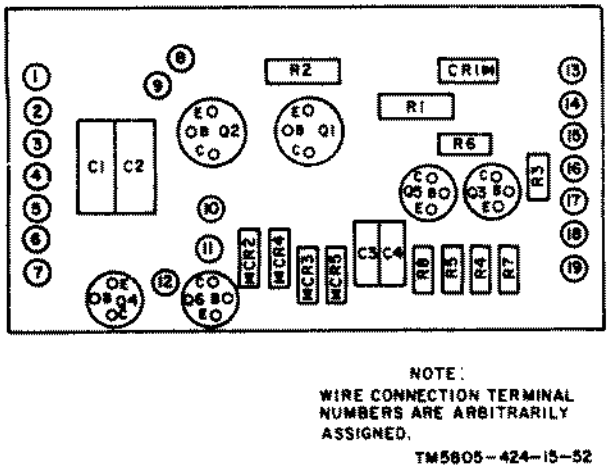


Figure 6-20. Printed-circuit card assembly A18A1A2 (PC 80034220), component location diagram.

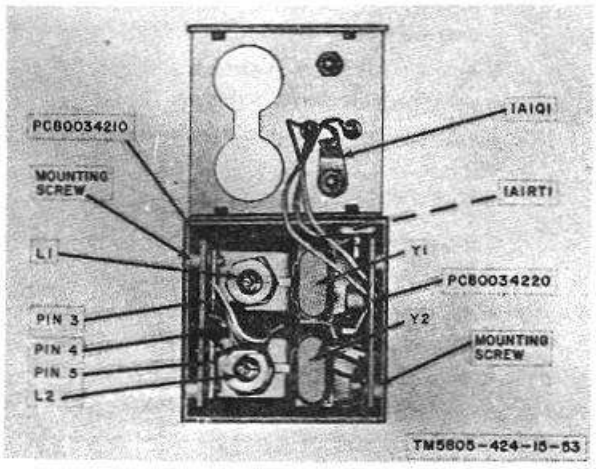


Figure 6-21. Crystal oscillator and oven assembly, cover removed.

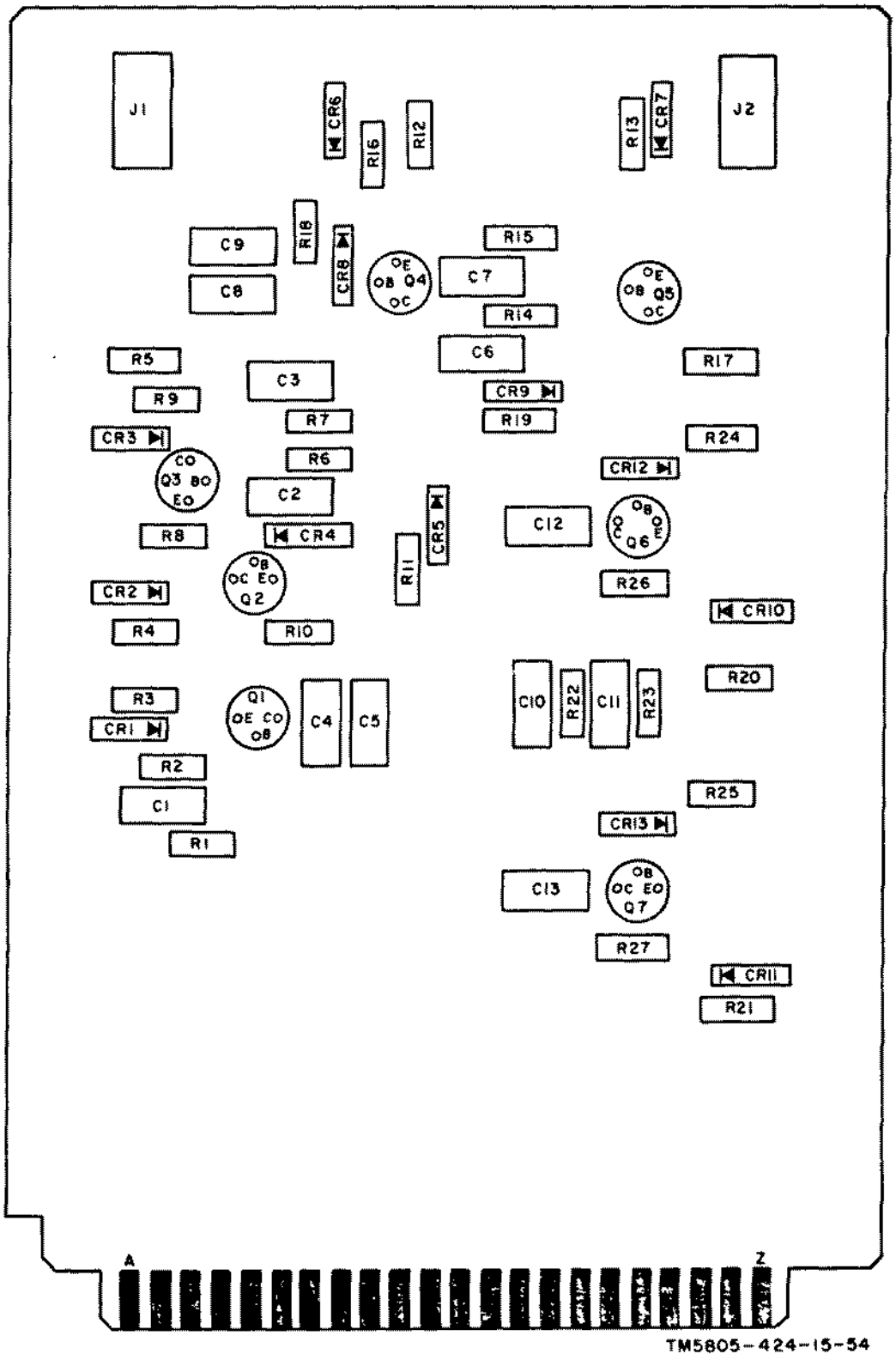


Figure 6-22. Printed-it card assembly A18A2, A19A2 (PC 80034200), component location diagram.

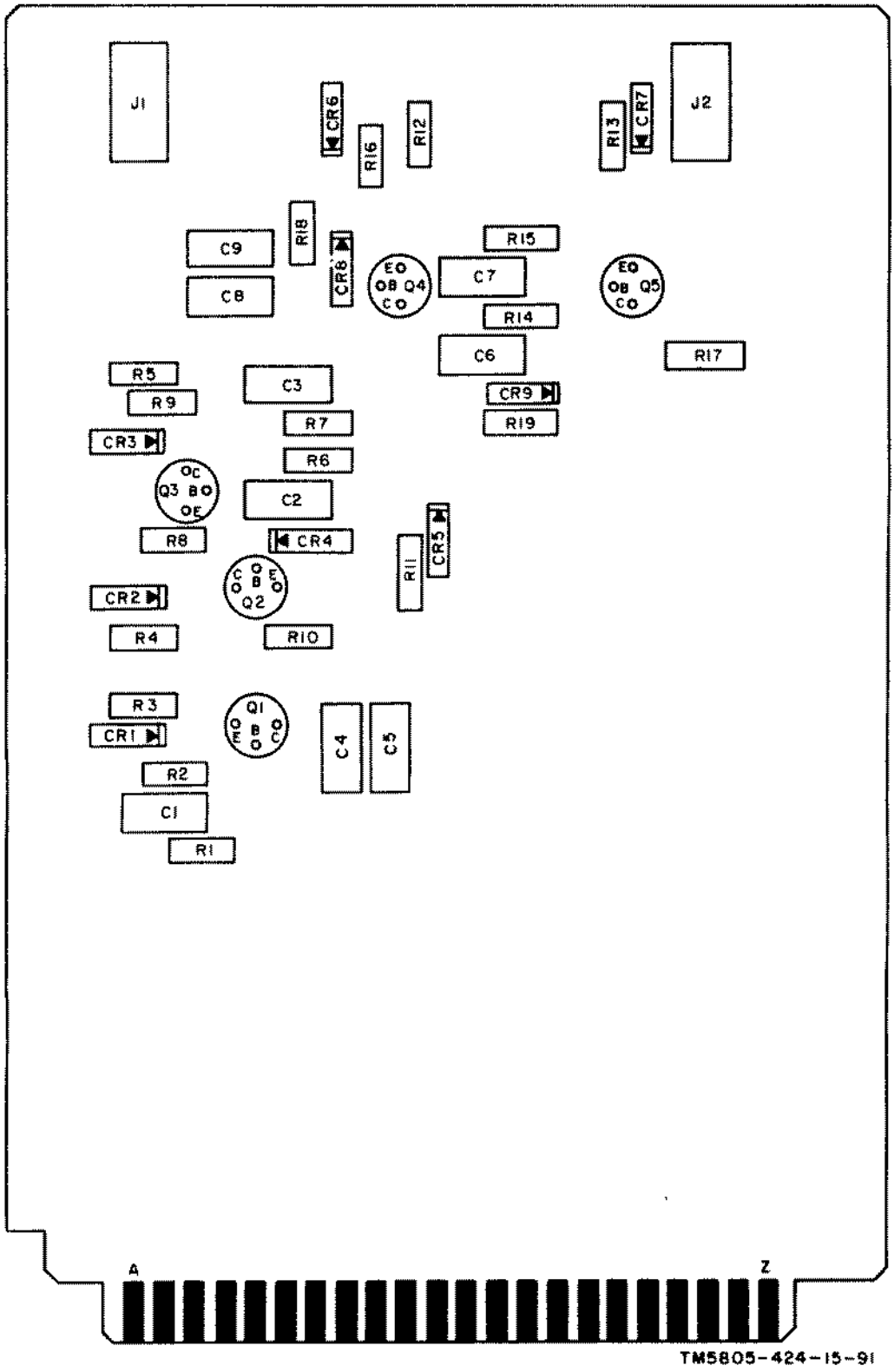


Figure 6-23. Printed-circuit card assembly A20A2, A21A2, A22A2 (PC 80034190), component location diagram.

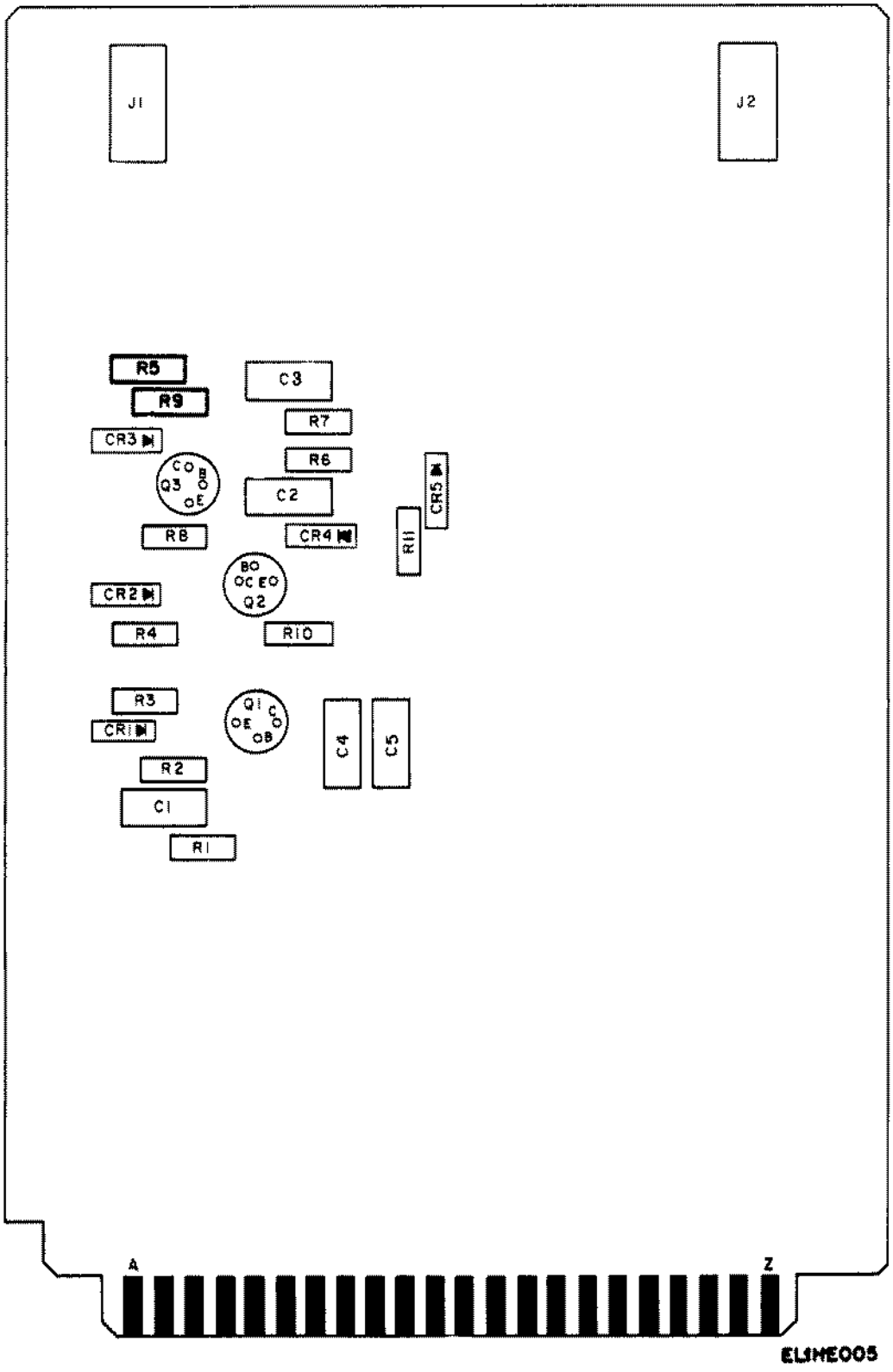


Figure 6-24. Printed-circuit card assembly A23A2 through A29A2 (PC 80034180), component location diagram.

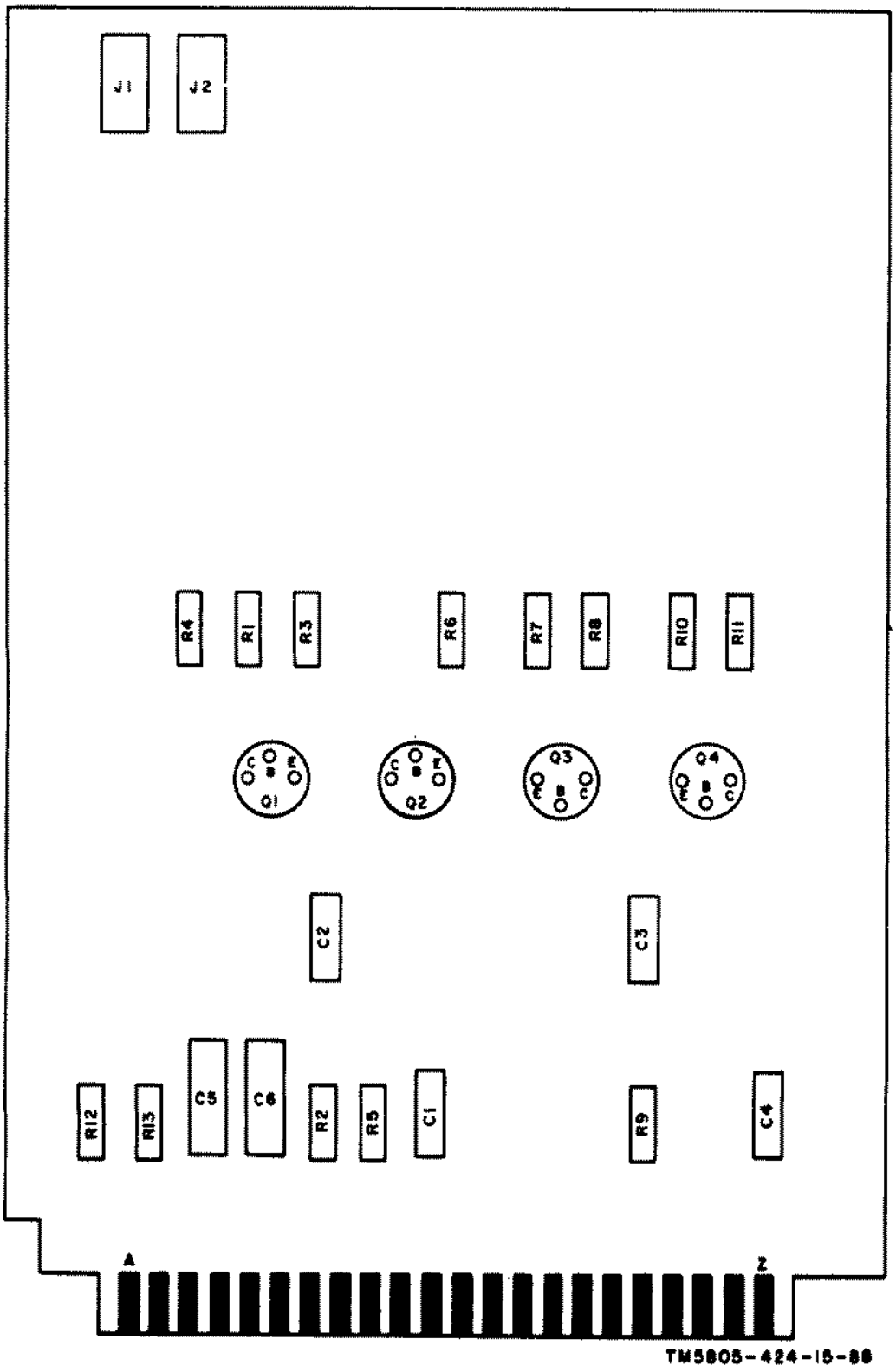


Figure 6-25. Printed-circuit card assembly A25A3 (PC 80034230), component location diagram.

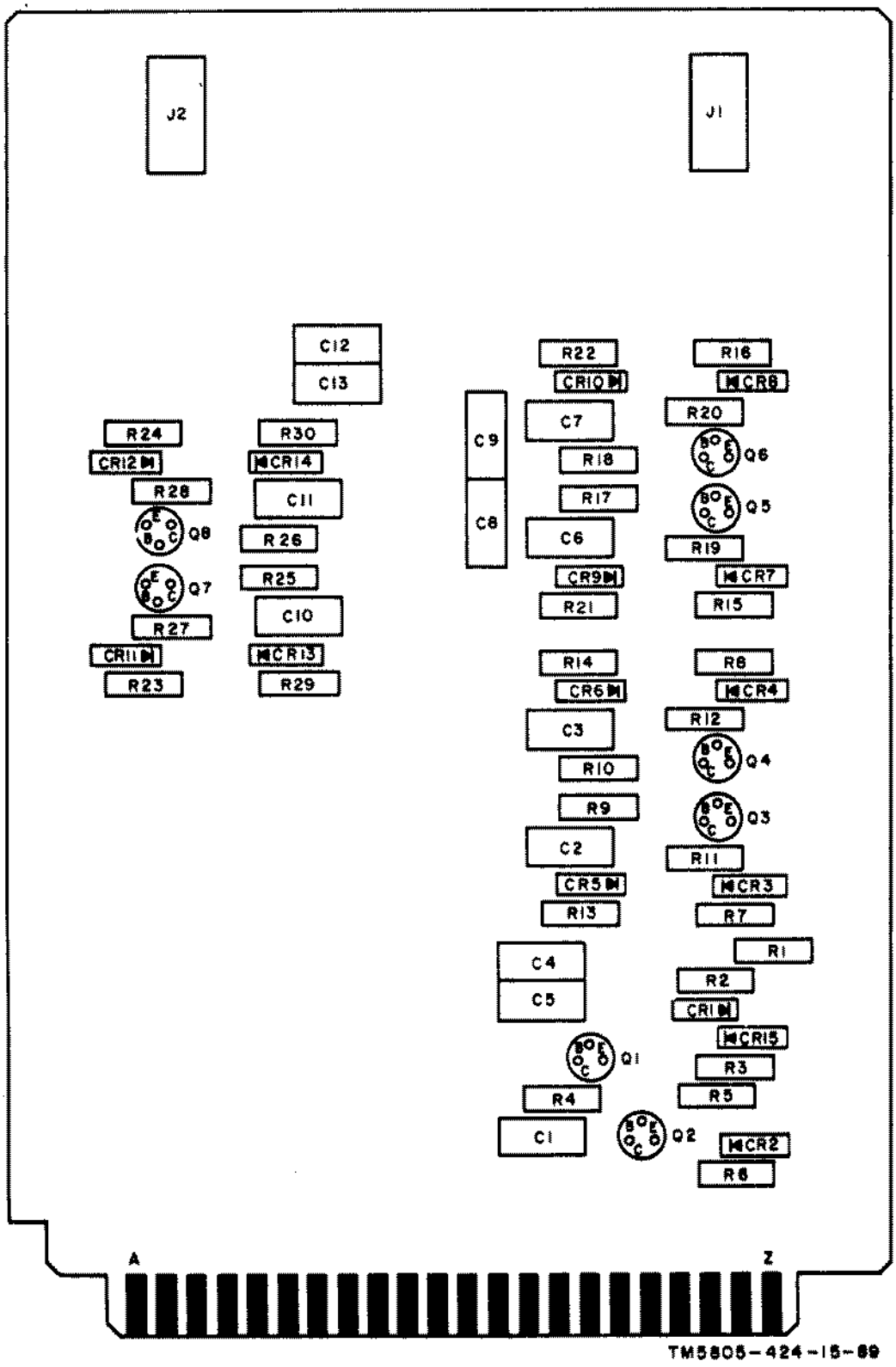


Figure 6-26. Printed-circuit card assembly A33A2 (PC 80034110), component location diagram.

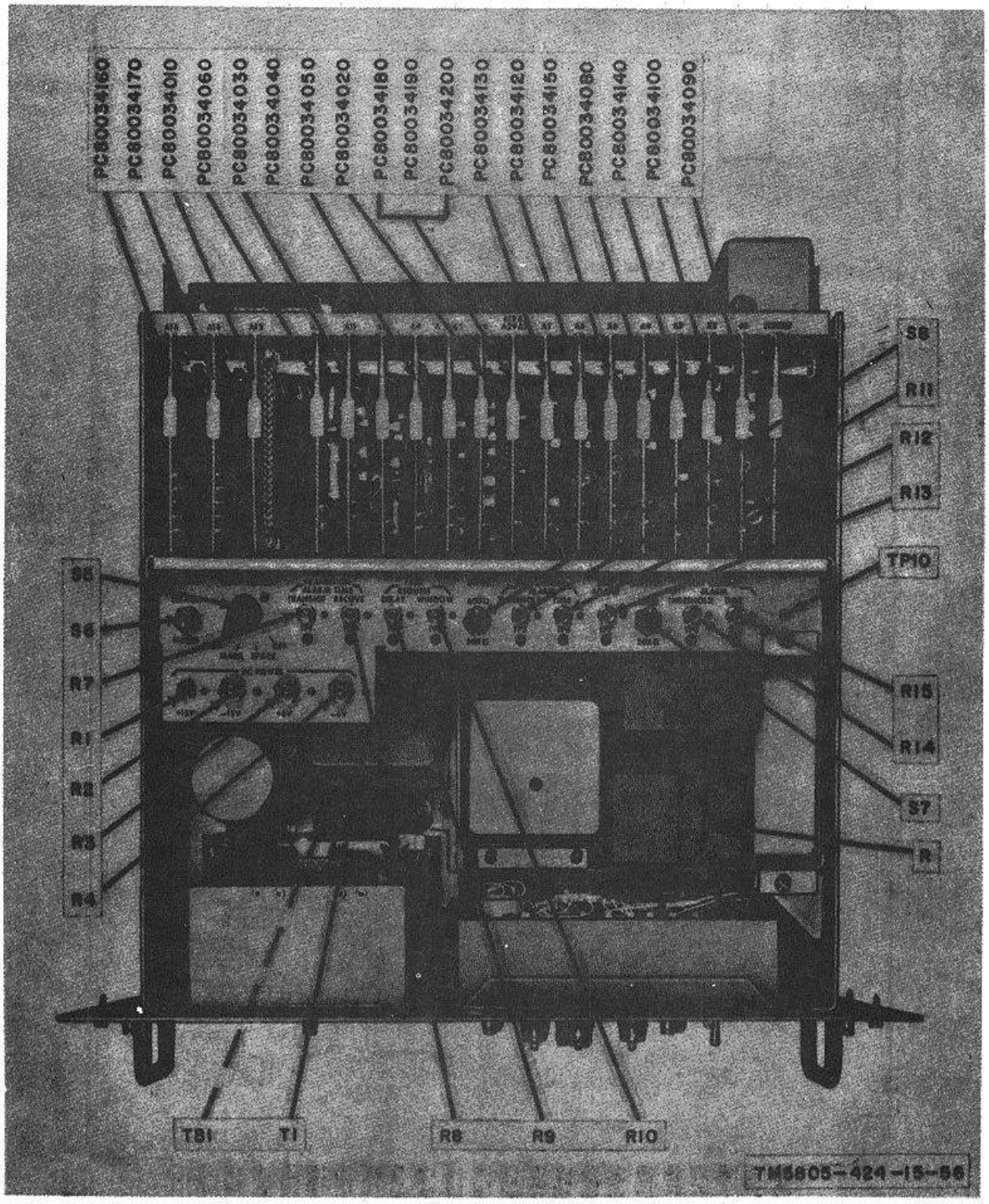


Figure 6-27. Modem, Low Speed Wire Line MD-674(P)/G, removed from case, top view.

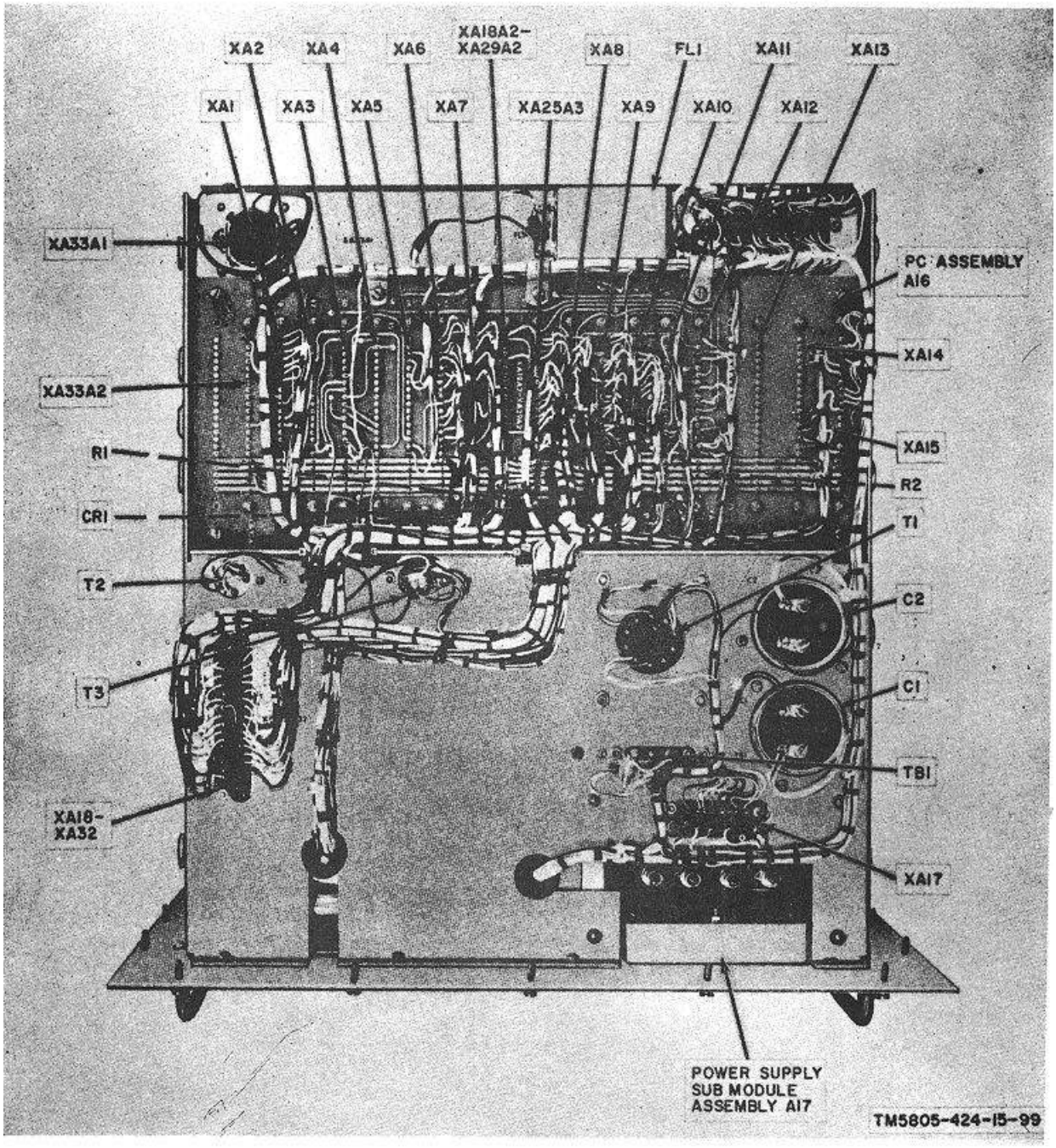


Figure 6-28. Modem, Low Speed Wire Line MD-674(P)/G, removed from case, bottom view.

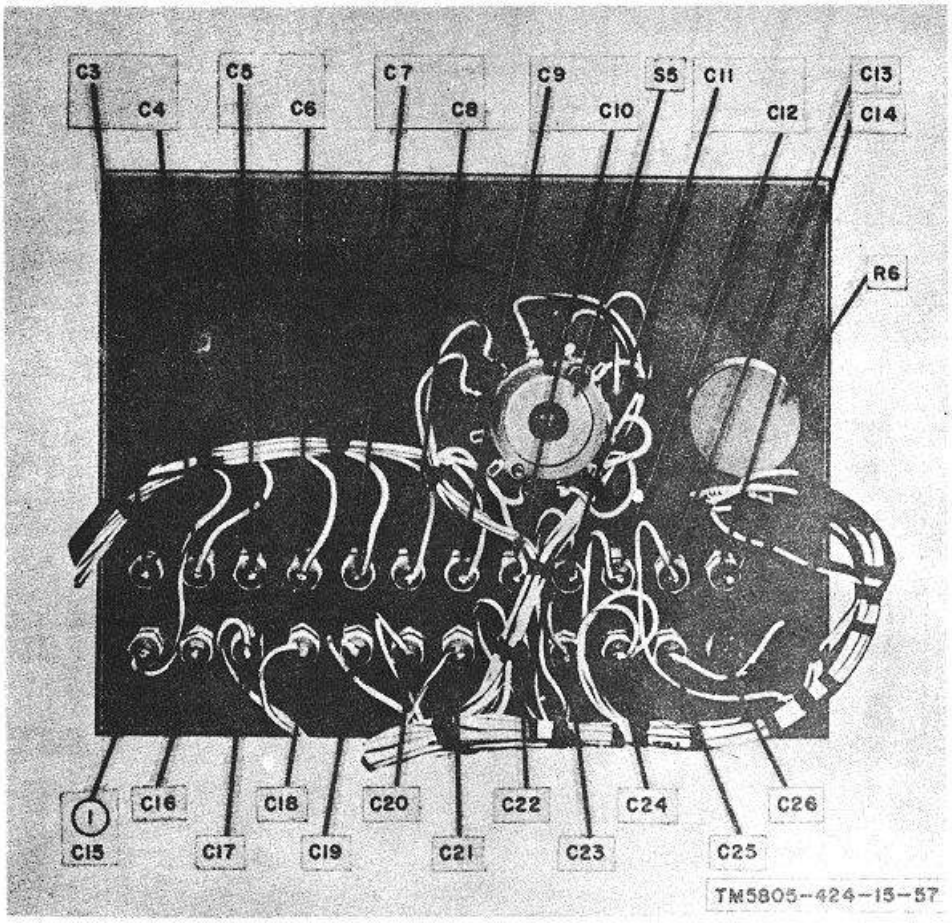


Figure 6-29. Modem, Low speed Wire Line 74 (P)/G, removed from, case, front panel, rear view.

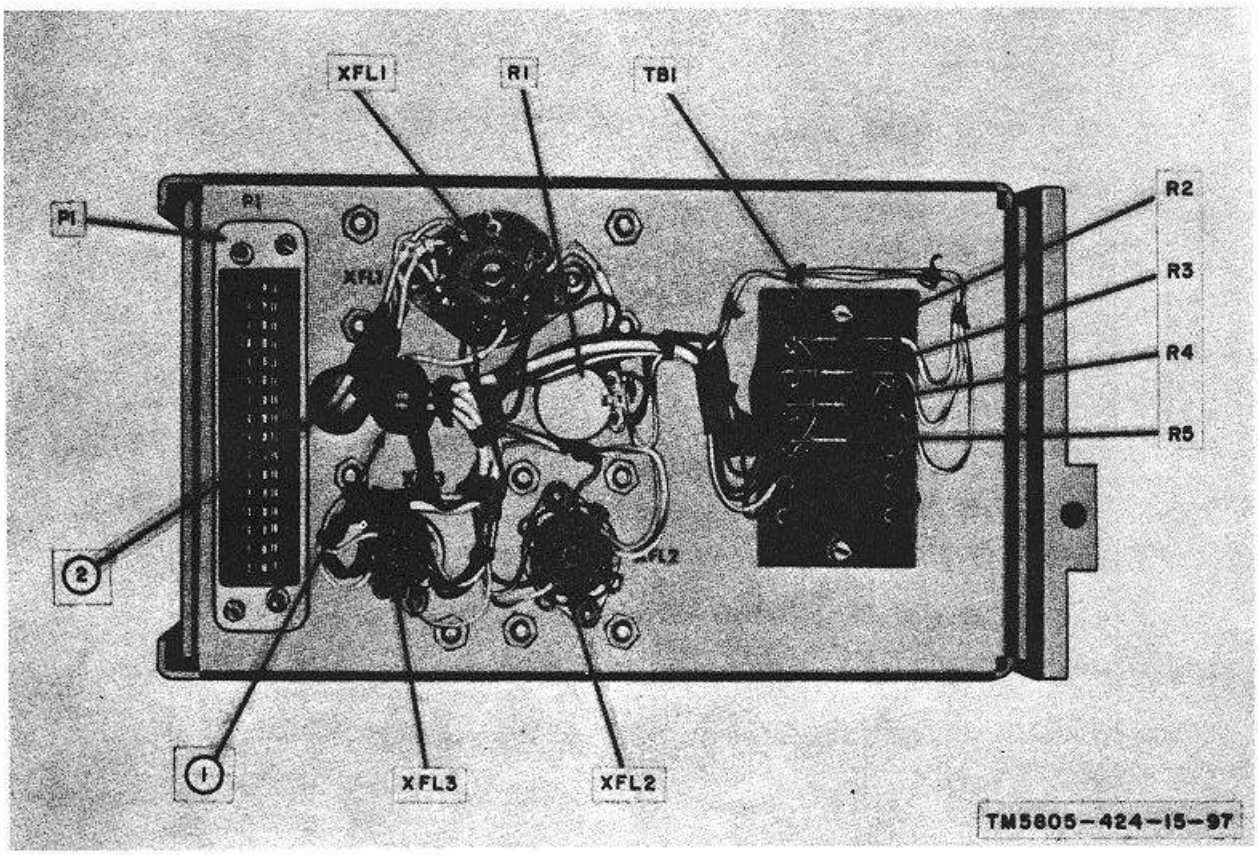


Figure 6-30. Plug-in module of Modem Subassembly MX-73(*)/G, bottom view.

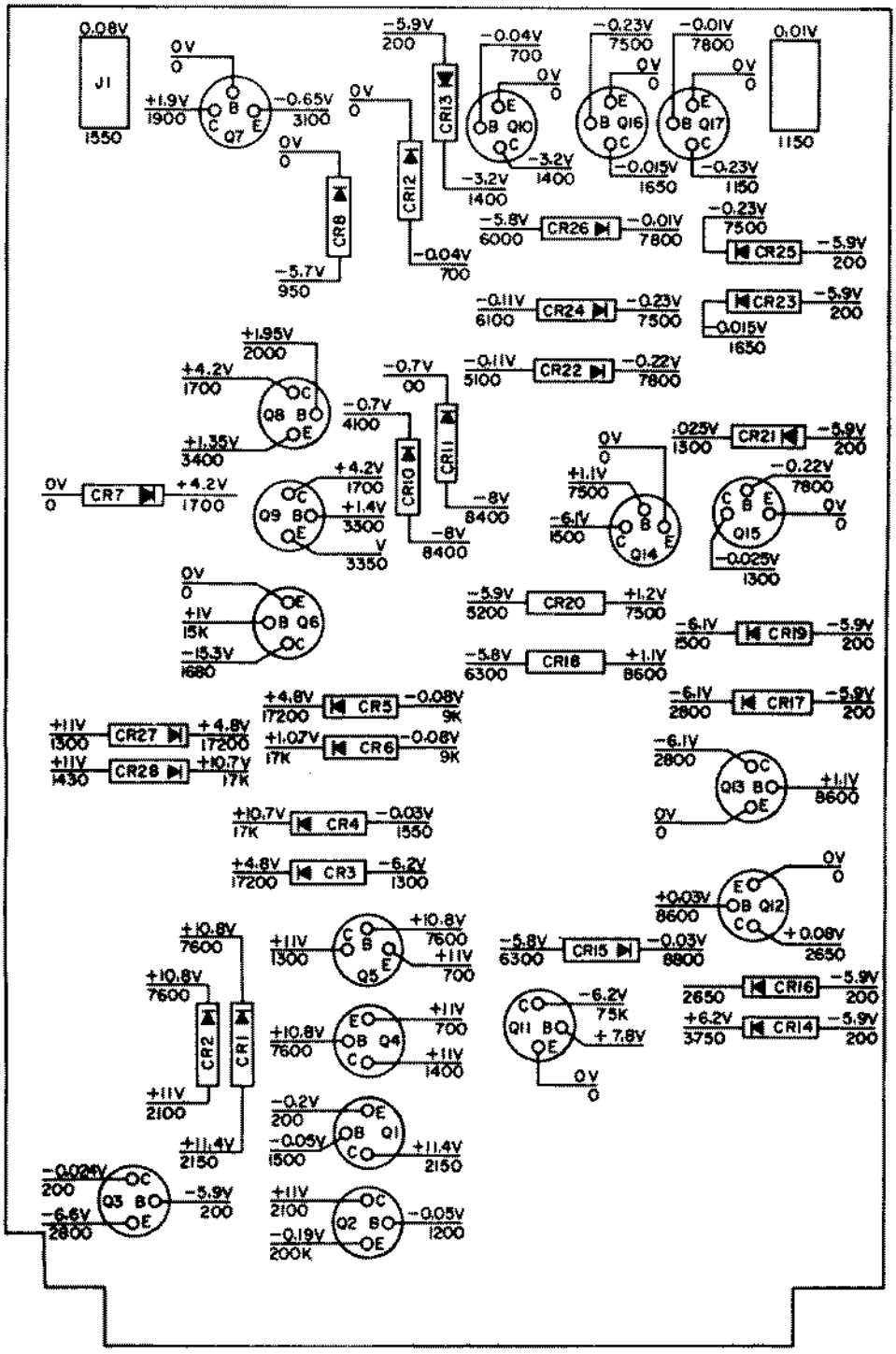
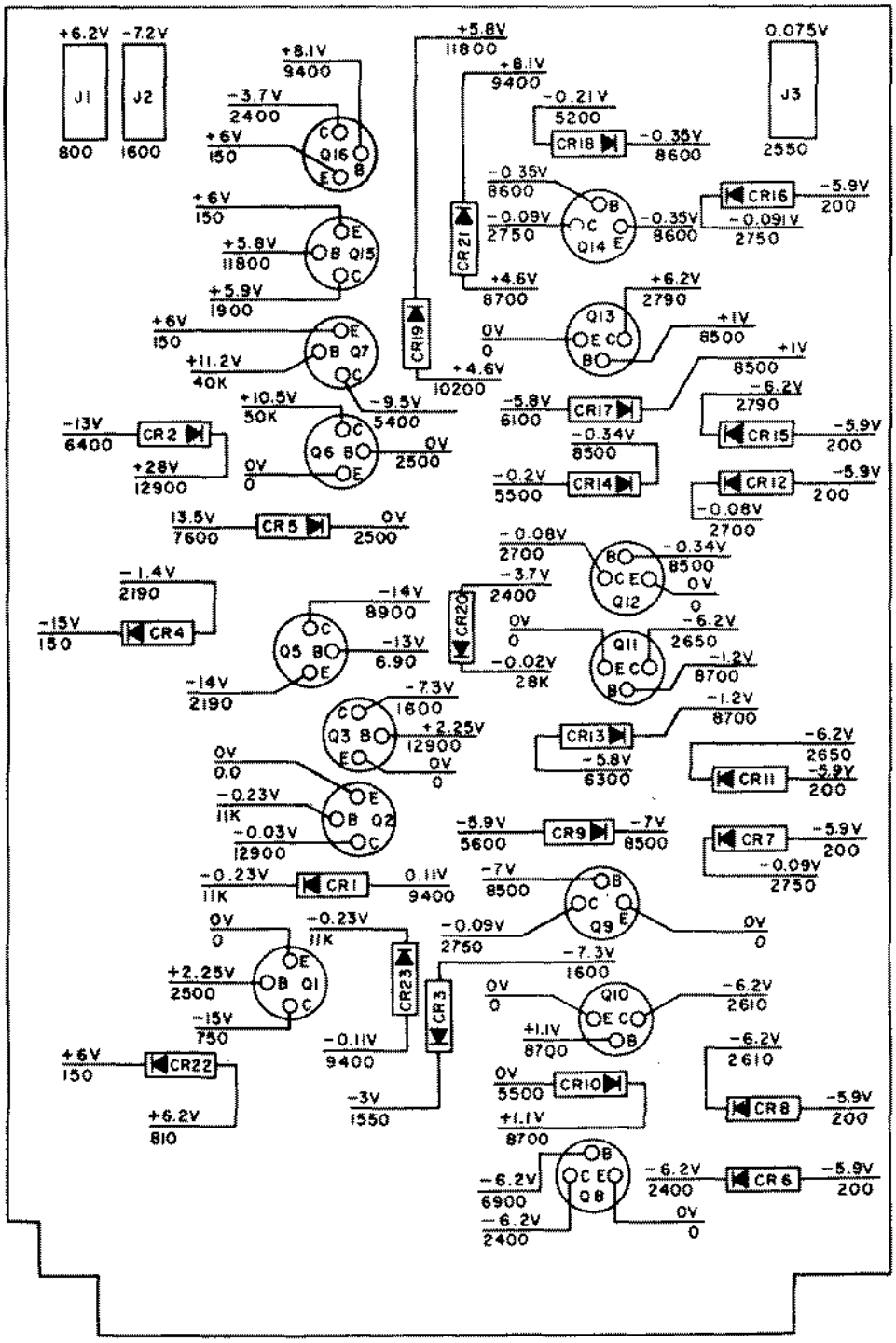


Figure 6-31. PC card assembly A1 (PC 80034090) voltage and resistance diagram.



NOTES:
1. VOLTAGE MEASUREMENT MADE WITH 20,000 OHMS-PER-VOLT METER.
2. UNLESS OTHERWISE SPECIFIED ALL RESISTANCES ARE IN OHMS.

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Figure 6-32. PC card assembly A3 (PC 80034140) voltage and resistance diagram.

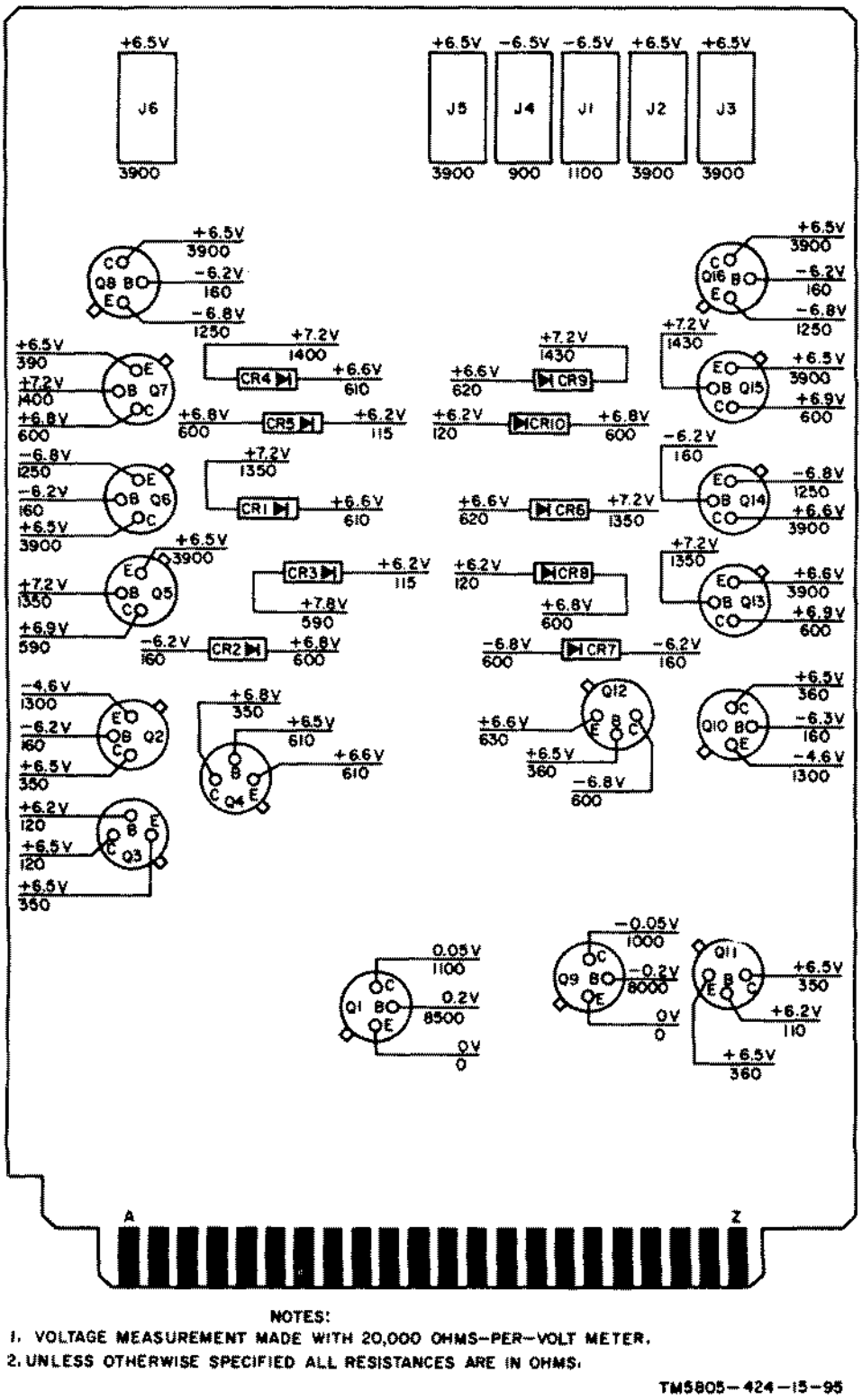
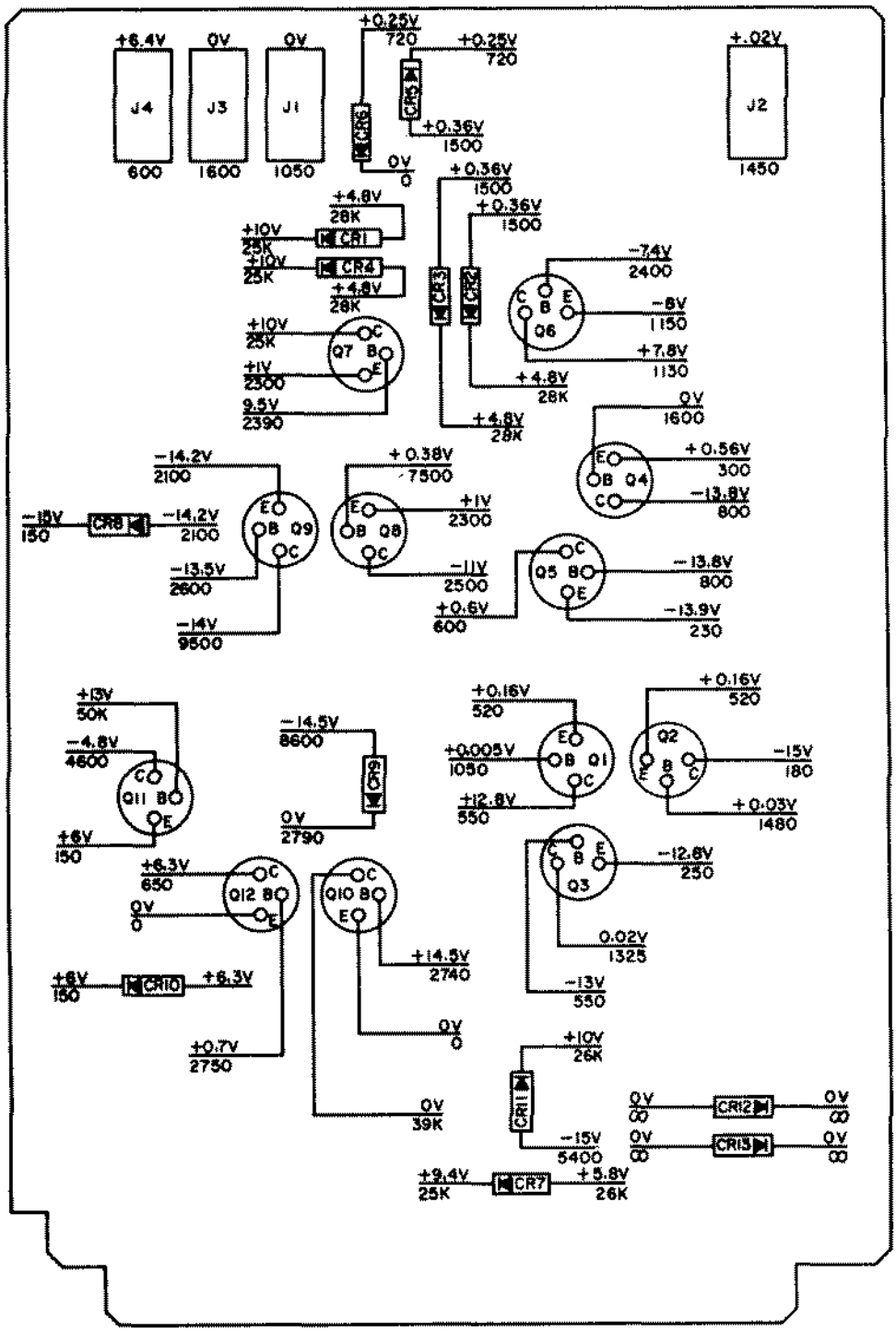


Figure 6-33. PC card assembly A5 (PC 80034150) voltage and resistance diagram.



NOTES:

1. VOLTAGE MEASUREMENT MADE WITH 20,000 OHMS-PER-VOLT METER.
2. UNLESS OTHERWISE SPECIFIED ALL RESISTANCES ARE IN OHMS.

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Figure 6-34. PC card assembly A6 (PC 80034130) voltage and resistance diagram.

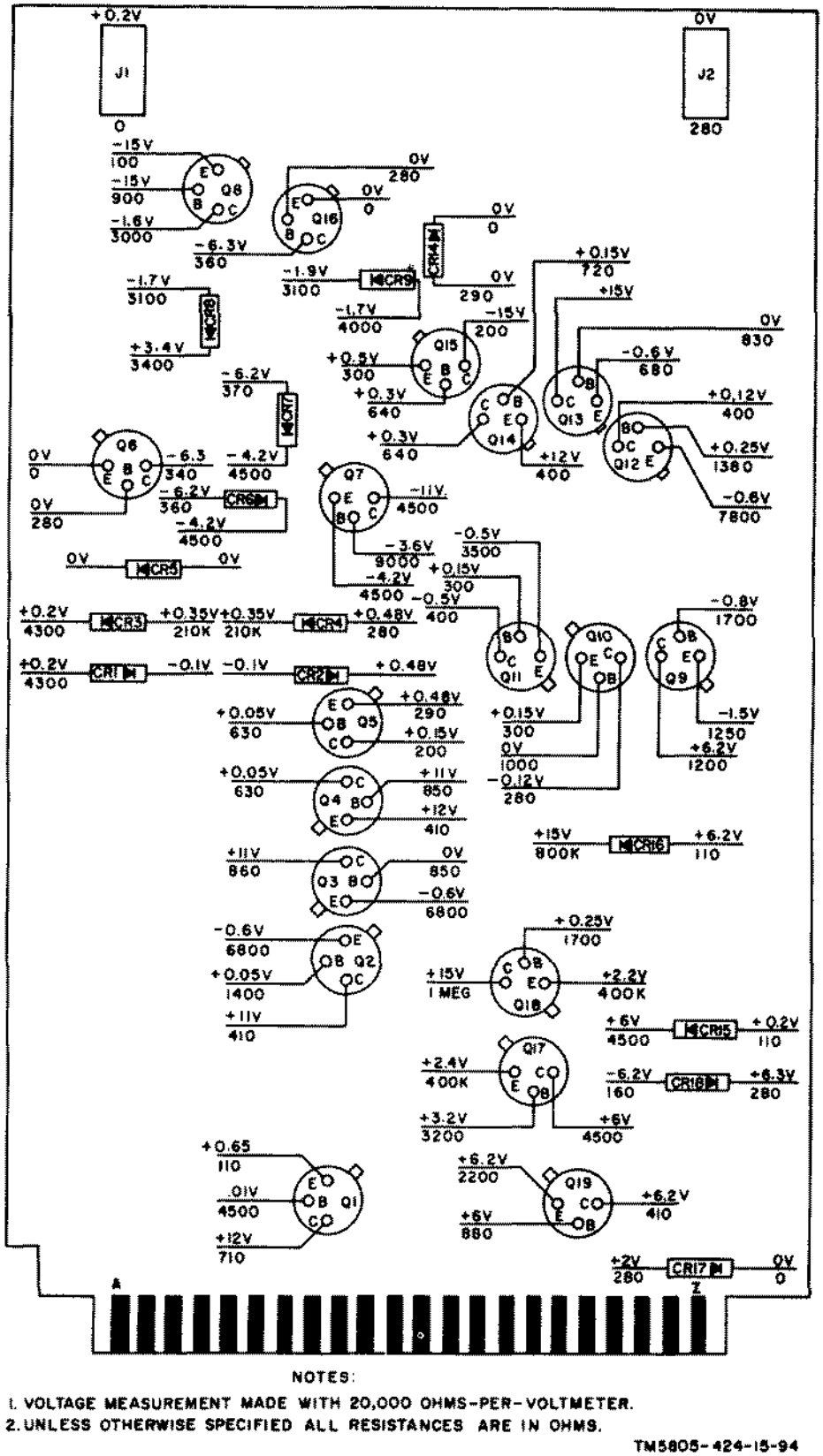


Figure 6-35. PC card assembly, A8 (PC 80034120) voyage and resistance diagram.

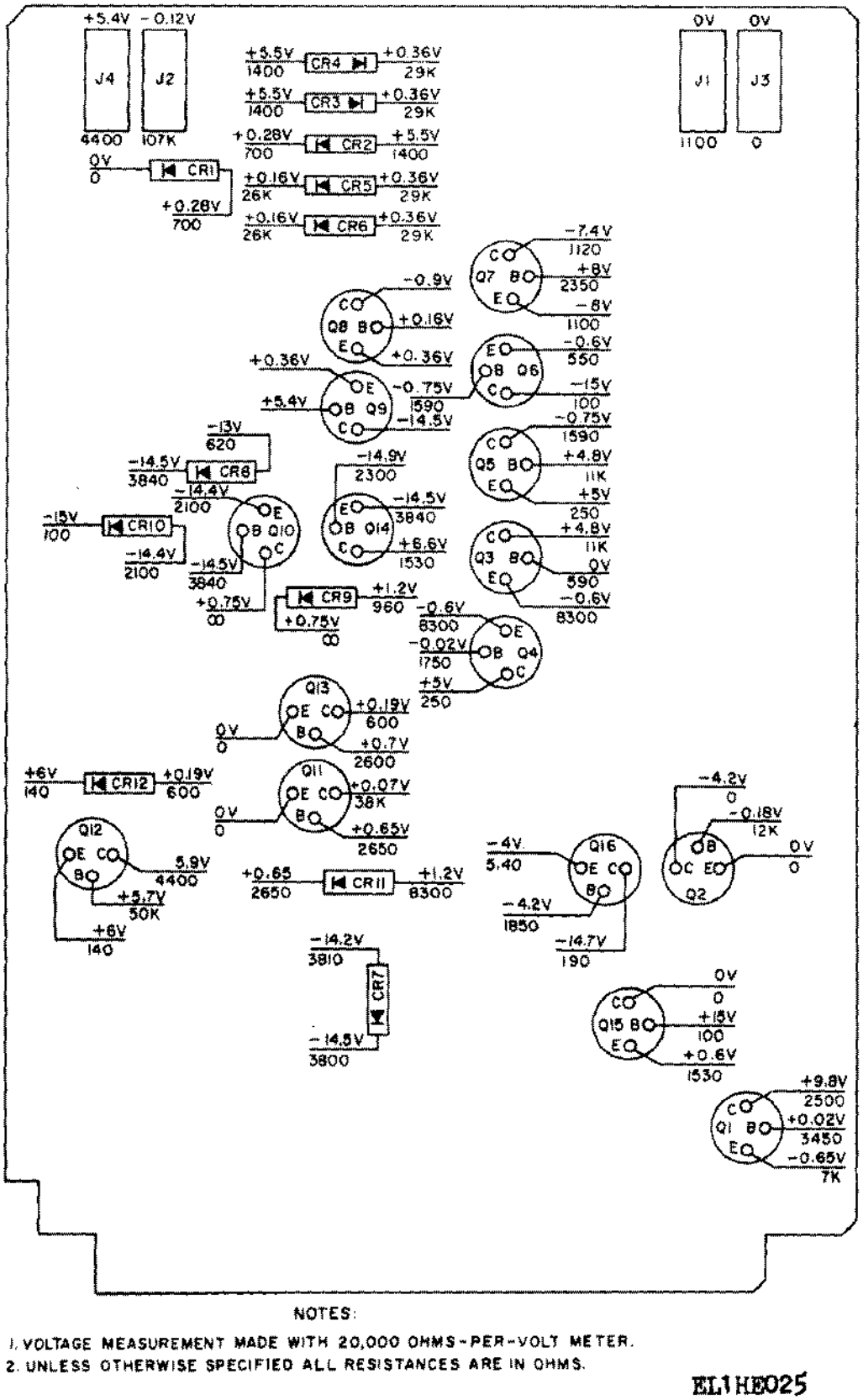
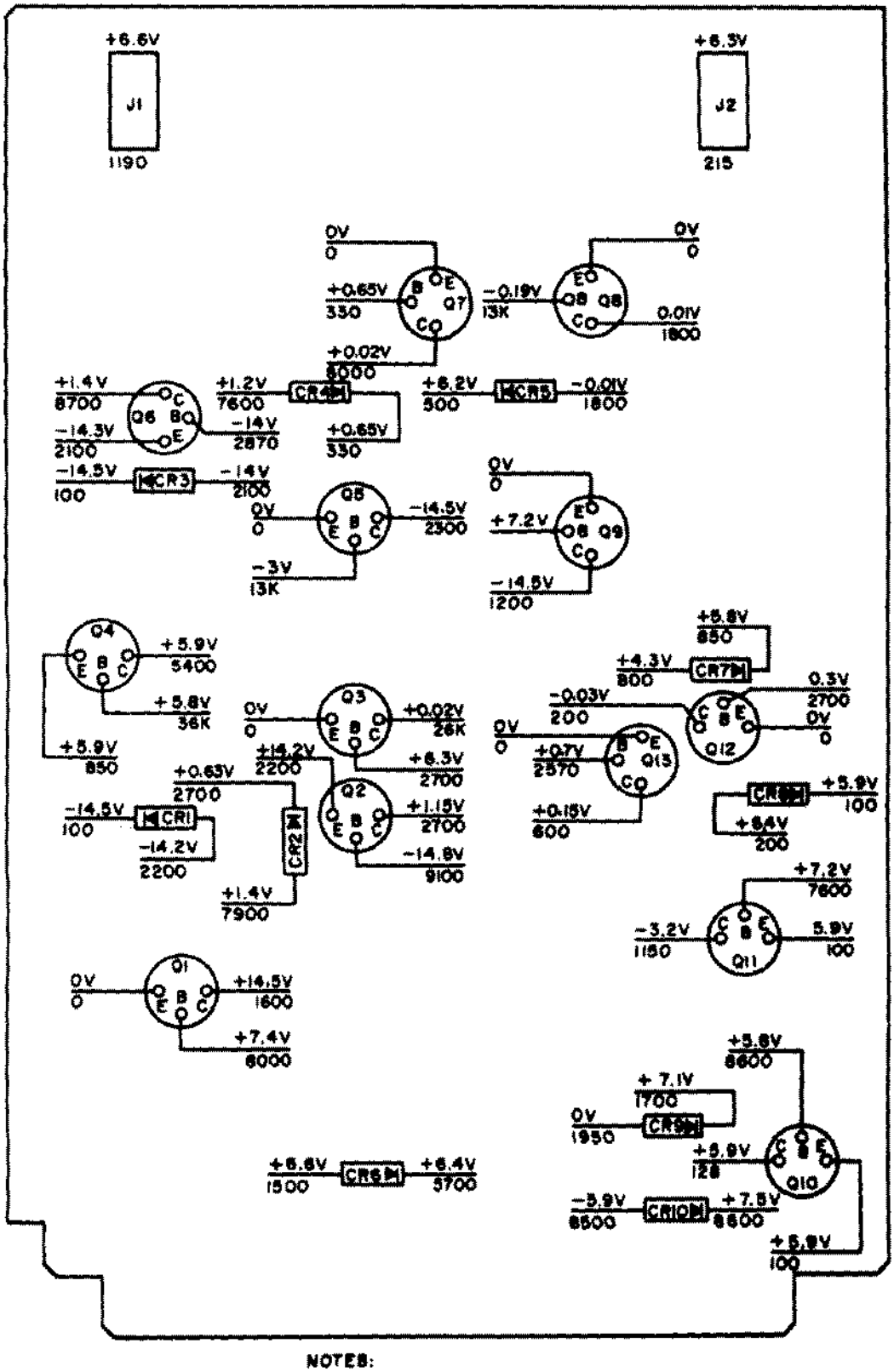


Figure 6-36. PC card assembly A9 (PC 80034050) voltage and resistance diagram.



NOTES:

1. VOLTAGE MEASUREMENT MADE WITH 20,000 OHMS-PER-VOLT METER.
2. UNLESS OTHERWISE SPECIFIED ALL RESISTANCES ARE IN OHMS.

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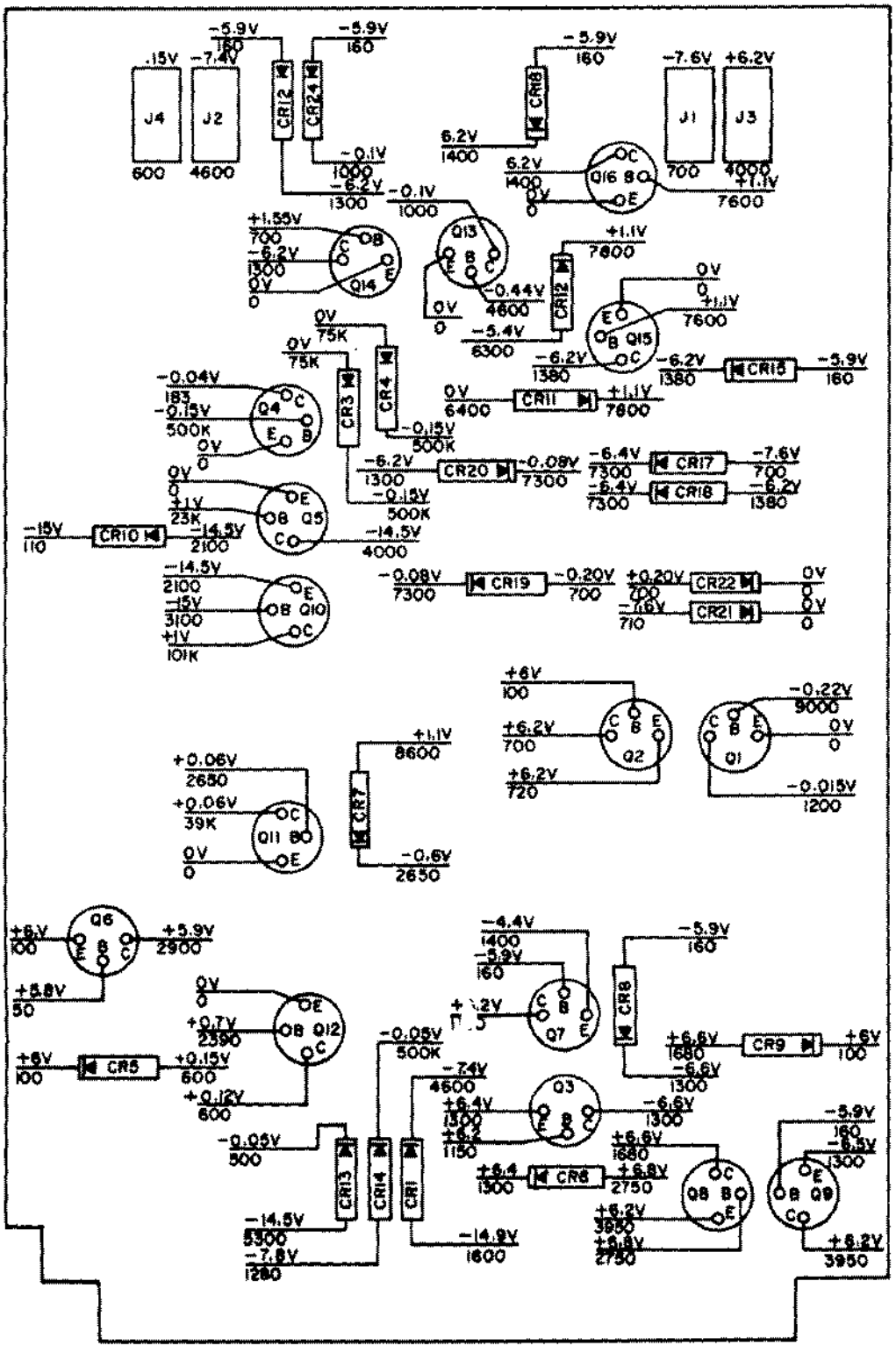
Figure 6-37. PC card assembly A10 (PC 80034040) voltage and resistance diagram.



NOTES:
1. VOLTAGE MEASUREMENT MADE WITH 20,000 OHMS-PER-VOLT METER.
2. UNLESS OTHERWISE SPECIFIED ALL RESISTANCES ARE IN OHMS.

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Figure 6-38. PC card assembly A11 (PC 80034030) voltage and resistance diagram.

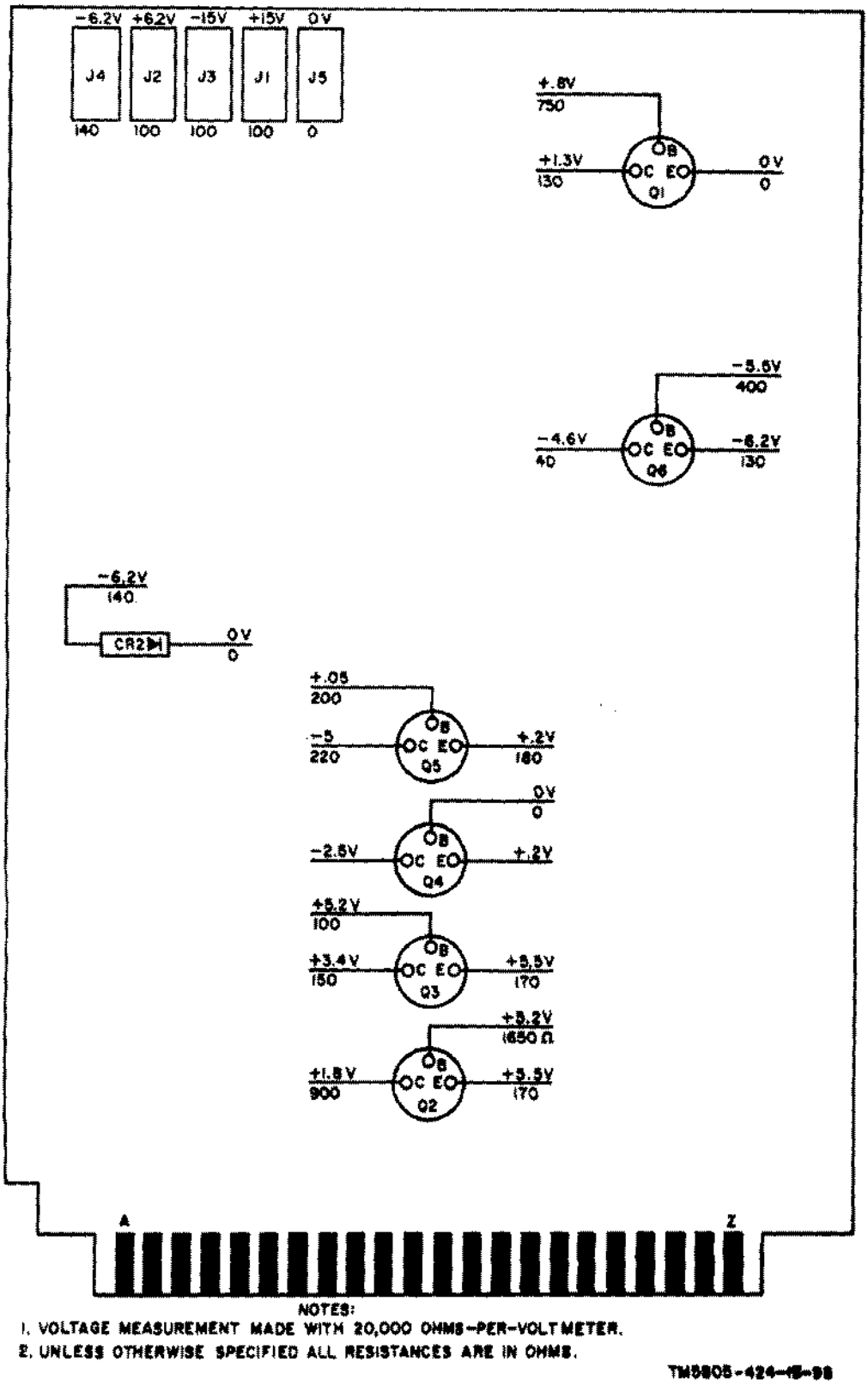
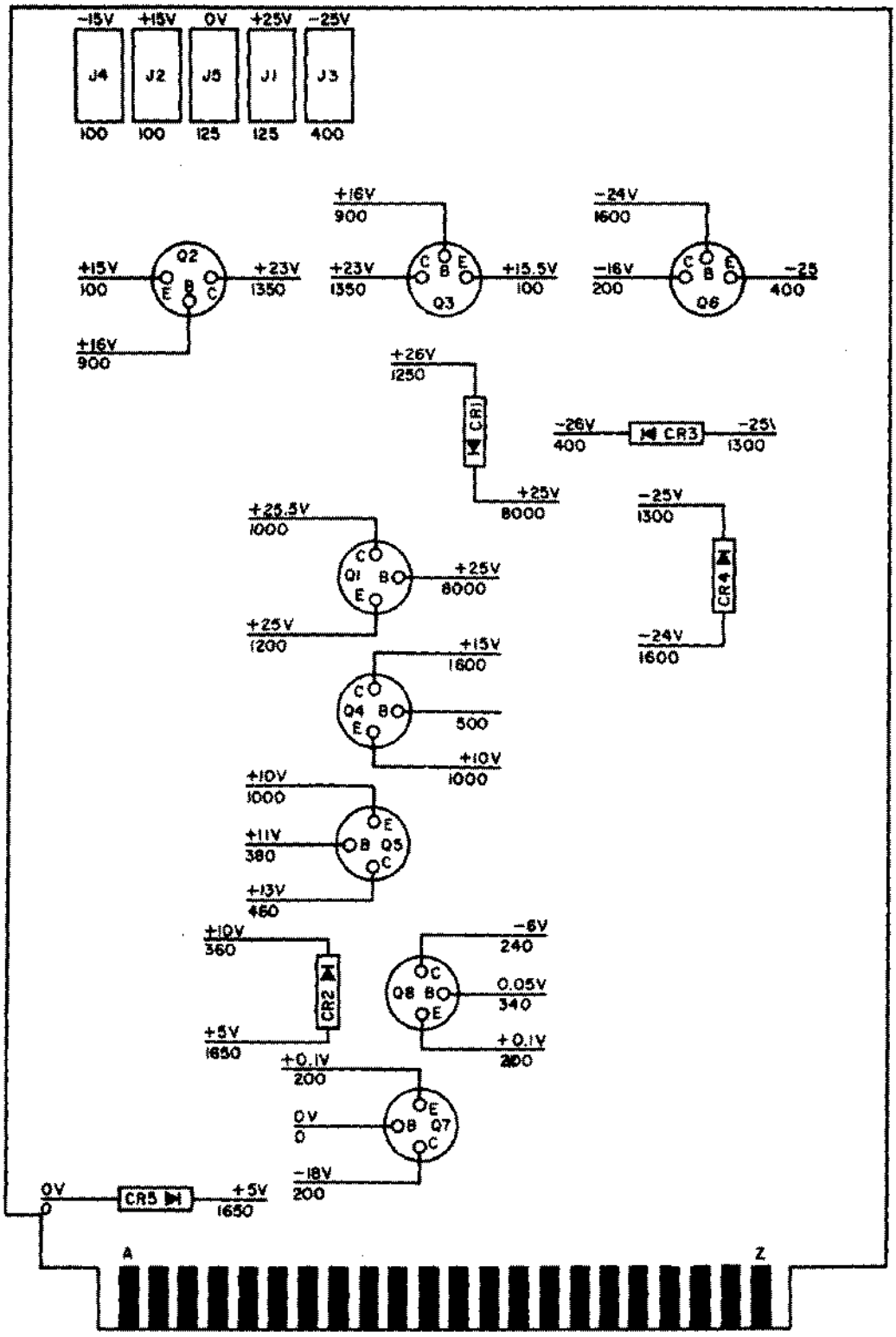


Figure 6-39. PC card assembly A14 (PC 80034170) voltage and resistance diagram.



NOTES:

1. VOLTAGE MEASUREMENT MADE WITH 20,000 OHMS-PER-VOLT METER.
2. UNLESS OTHERWISE SPECIFIED ALL RESISTANCES ARE IN OHMS.

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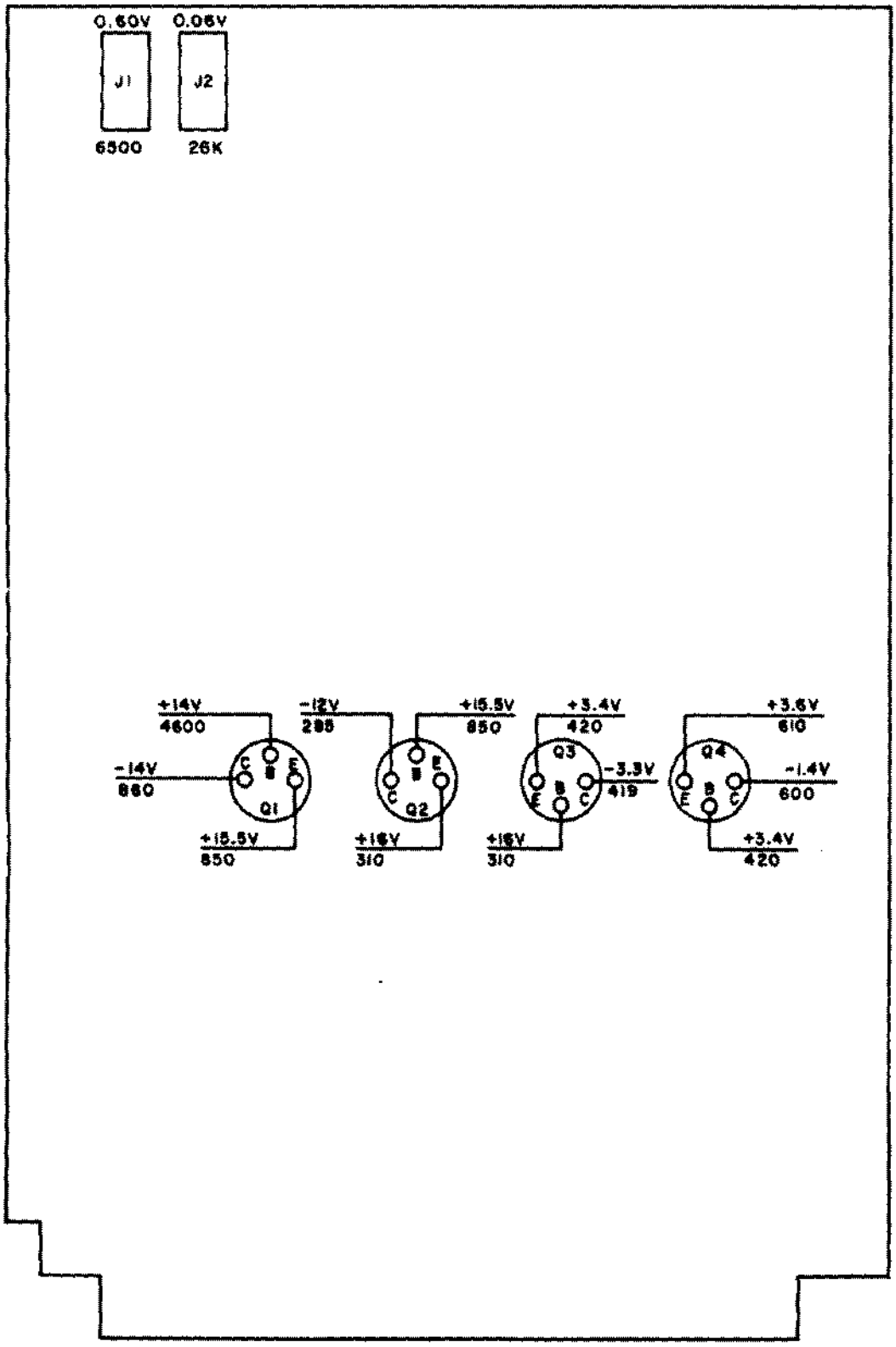
Figure 6-40. PC card assembly A15 (PC 80034160) voltage and resistance diagram.



NOTES:
1. VOLTAGE MEASUREMENT MADE WITH 20,000 OHMS-PER-VOLT METER.
2. UNLESS OTHERWISE SPECIFIED ALL RESISTANCES ARE IN OHMS.

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Figure 6-41. PC card assembly A25A3 (PC 80034230) voltage and resistance diagram.

6-4. Localizing Troubles

a. General. The following procedures are to be used to localize troubles when abnormal indications are obtained during the operational tests (para 6-3), or when Symptoms of abnormal operation are indicated by operating or organizational maintenance personnel. Certain results obtained during this procedure localize the trouble to a particular component. However, in general, the procedure localizes the trouble to a specific logic circuit or to a small group of logic circuits.

The trouble is then localized to a component or connection by use of the isolation procedures (paras 6-5, 6-, and 6-7), the timing waveforms (fig 5-8 and 5-9), the printed-circuit board layout diagrams (figs. 6-2 through 6-26), component location illustrations (figs 6-27 through 6-30), the schematic diagrams (figs. 8-6 through 8-27), and the wiring diagrams (figs. 6-43 through 6-46, and fig. 8-28).

b. Use of Troubleshooting Chart. The troubleshooting chart (*b* below) is used by checking the *Symptom* column for abnormal operation. The Probable trouble column characterises the nature of the trouble. The Corrective measure column indicates the circuits or circuit elements to be checked, or references a troubleshooting procedure when further troubleshooting steps are necessary.

Note. The probable trouble and corrective measures indicated below do not Include the possibility of defective wiring. When the trouble cannot be repaired using the corrective measures Indicated, check the wiring associated with the particular circuit and repair any defective wiring.

c. Troubleshooting Chart.

Item No.	Symptom	Probable trouble	Corrective measure
1	AC POWER indicator lamp does not light with AC POWER switch at ON.	*a*. Defective ac line filter FL1 (fig. 6-28).	*a.* Check for input ac voltage at output terminals of line filter; replace filter, if defective (par 6-8).
		b. Defective AC POWER switch S1 (fig. 8-28).	*b.* Check for as voltage across pins 1 and 4 of transformer TI (fig. 6-28). Replace switch if voltage is not present (para 6-8*a*).
		c. Defective power transformer T1 (fig. 6-28).	*c*. Check voltage and resistance across pins 9 and 10 and 9 and 11 of transformer T1 (fig. 6-42); replace transformer, if defective.
		d. Defective feedthrough capacitors 2A1C10, 2A1C111, 1A1C3, 1A1C6, or resistor 1A1R5 (fig. 6-28); defective fuse holder.	*d.* Check continuity of components; replace defective part (para 6-8*a*).
2	MD-674(P)/G is completely inoperative, AC POWER Indicator lamp lights.	*a*. Defective filter capacitor C1 or C2 (fig. 6-28).	*a*. Check capacitors (fig. 6-42); replace, if defective (par 6-8*a*).
		b. Defective feedthrough capacitor 1A1C7 or 1A1C10 (fig. 6-29).	*b.* Check capacitors; replace defective component (para 6-8*a*).
		c. Defective power transistor or rectifiers on the power supply sub-module (fig. 6-28).	*c*. Make voltage and resistance measurements of power supply sub module components (fig. 6-18); replace defective components (par 6-8*b*).
3	Blower does not operate----------	Defective fan motor BI (fig. 6-18) ----------	Replace fan assembly (para 6-8*b*).
4	No transmit data supplied by MD-674(P)/G.	*a.* Defective INPUT SELECT switch (fig. 2-3).	*a*. Check switch continuity (fig. 6-29); replace switch if defective (para 6-8*a*).
		b. Defective output transformer T2 (fig. 6-28).	*b*. Check transformer voltage and resistances (fig. 6-42); replace transformer, if defective.
		c. Shorted ORDER WIRE SEND jack J1 (fig. 3-1).	*c.* Check jack; replace, if defective (fig. 8-28).

c. Troubleshooting Chart-Continued

Item No.	Symptom	Probable trouble	Corrective measure
4	No transmit data supplied by MD-674(P)/G-Con.	d. Shorted LINE MONITOR SEND jack J3.	d. Check jack; replace, if defective (fig. 8-28).
		e. Defective OUTPUT LEVEL ADJ control R6.	e. Check control resistance (fig. 6-29); replace control, if defective (fig. 8-28).
5	No receive data supplied by MD-674(P)/G.	a. Defective input transformer T3 (fig. 6-28).	a. Check transformer voltage and resistance (fig. 6-42); replace transformer, if defective.
		b. Shorted ORDER WIRE RECEIVE jack J2 (fig. 3-1).	b. Check jack; replace, if defective (fig. 8-28).
		c. Shorted LINE MONITOR RECEIVE jack J4.	c. Check jack; replace, if defective (fig. 8-28).
6	Send transition alarm cannot be activated or is always activated.	Defective TRANSMIT TRANSITION ALARM TIME resistor R7 (fig. 2-3).	Check resistor; replace, if defective (fig. 8-28).
7	Send carrier alarm cannot be activated or is always activated.	Defective XMIT CARRIER ALARM THRESHOLD R14 or TIME R15 resistor.	Check resistors; replace defective component (fig. 8-28).
8	Receive transition alarm cannot be activated or is always activated.	Defective RECEIVE TRANSITION ALARM TIME resistor R8.	Check resistor; replace, if defective (fig. 8-28).
9	Receive carrier alarm cannot be activated or is always activated.	Defective REC CARRIER ALARM' THRESHOLD R11 or TIME R12 resistor.	Check resistors; replace defective components (fig. 8-28).
10	Loss-of-transmit-carrier alarm activated when INPUT SELECT switch is set to MARK only.	*a*. Defective mark oscillator on PC 80034210 (fig. 6-21).	*a*. Check for output frequency at pin 3 of PC 80034210 (fig. 6-19). If not present, check capacitors C1 through C5, inductor L1, resistors R1, R2, and R3, and transistors Q1 and Q2 (fig. 8-21); replace defective components.
		b. Defective crystal Y1	*b*. Replace crystal Y1.
		c. Defective amplifier AM-1 on PC 80034220.	*c*. Check amplifier stage (para 6-7*b* and fig. 8-21); replace defective components.
		d. Defective AND gate GAI-1 on PC 80034220.	*d*. Check AND gate (para 6-6*a* and fig. 8-21); replace defective components.
11	Loss of-transmit-carrier alarm activated when INPUT SELECT switch is set to SPACE only.	*a*. Defective space oscillator on PC 80034210 (fig. 6-21).	*a*. Check for output frequency at pin 4 of PC 80034210 (fig. 6-19). If not present, check capacitors C6 through C10, inductor L2, resistors R5, R6, and R7, and transistors Q3 and Q4 (fig. 8-21); replace defective components.
		b. Defective crystal Y2	*b*. Replace crystal Y2.
		c. Defective amplifier AM-2 on PC 80034220 (fig: 6-21).	*c*. Check amplifier stage (para 67*b* and fig. 8-21); replace defective component.
		d. Defective AND gate GAI-2 on PC 80034220.	*d*. Check AND gate (para 6-6*a* and fig. 8-21); replace defective components.

c. Troubleshooting Chart - Continued

Item No.	Symptom	Probable trouble	Corrective measure
12	Loss-of-transmit-carrier alarm activated with INPUT SELECT switch in any position.	a. Defective INPUT SELECT switch 1A1S5 (fig. 2-3).	a. Check switch; replace, if defective (fig. 8-28).
		b. Defective ORDER WIRE SEND jack J1(fig. 3-1).	b. Check jack; replace, if defective (fig. 8-28).
		c. Defective feedthrough capacitor C10, C17, or C18 (fig. 6-29).	c. Check capacitors; replace, if defective (fig. 8-28).
		d. Defective amplifier DIA-1 on PC assembly A12 (fig. 8-17). defective components (fig. 6-13).	d. Take voltage and resistance measurements of Q 1-Q4 circuitry; replace
		e. Defective circuit in transmit section:	c. Troubleshoot transmit section as follows:
		(1) Defective frequency divider module PC assembly A18A2-A32A2 (if used) (fig. 8-22, 8-23, or 8-24).	(1) Check for square wave output at test jack J2 on PC 80034200 (fig. 6-22), PC 80034190 (fig. 6-23); PC 80034180 (fig. 6-24); if not present, troubleshoot countdown chain FFC-1, FFC-2, and FFC-3 (para 6-5), and amplifier IN-1 (para 6-7a); replace defective components.
		(2) Defective 64 divider module assembly A7 (fig. 812).	(2) Check for square wave output at test jack J2 on PC 80034130 (fig. 6-8). If not present, check for square wave at TP6 through TP1, in turn, and troubleshooting countdown chain FFC-4 through FFC-9 (para 6-5), respectively. If no output is present at TP1, check amplifier IN-2 (para 6-7a). If output is present at J2, check amplifiers AM-3, AM-4, and PSA-1 (para 6-7b).
		(3) Defective transmit filter FL2 (fig. 2-6).	(3) Check for output at pins 8 and 10 of connector A18PI-A32PI of MX-73(*)/G (fig. 6-28). If no output is present, replace FL2.
		(4) Defective resistor AIR16 (fig. 8-28).	(4) Check resistor; replace, it defective (fig. 8-28).
		(5) Defective OUTPUT LEVEL ADJ resistor 1AIR6 (fig. 3-1).	(5) Check resistor; replace, if defective (fig. 8-28).
		(6) Defective output amplifier Q1, Q2, Q3 on assembly A6 (fig. 8-11).	(6) Check for output signal at test jack J2 on PC 80034120 (fig. 6-7). If present, check transformer 1AIT2 (fig. 6-34); replace, if defective. If no output at J2, check voltage and resistance of output amplifier circuit (Q1, Q2, Q3, fig. 68-34); replace defective components.
		(7) Defective diode CR12 or CR13 on assembly A6 (fig. 8-11).	(7) Check diode voltage and resistance (fig. 6-34); replace diode, if defective.

c. Troubleshooting Chart-Continued

Item No.	Symptom	Probable trouble	Corrective measure
12	Loss-of-transmit-carrier alarm activated with INPUT SELECT switch in any position-Continued	*f.* Defective bistable FFE-1 or OR gate GOA-6 on assembly A3 (fig. 8-8).	*f.* Check output voltage at test jack J2 of PC 80034140 (fig. 6-4). If output is positive (ground), troubleshoot FFE-1 (para 6-5) and GOA-6 (para 6-6d); replace defective components.
13	No-transition send alarm activated; send output normal.	Defective alarm circuit on assembly A12 (fig. 8-17); defective delay driver Q5, Q6, Q7.	Check for ground at TP1 of PC 80034060 (fig. 6-13). If not present, check AND gates GAS-1 and GAS-2 (para 6-6*b*). If present, check for - 15 volts at TP2; if present, check delay driver components (fig. 8-7 and 6-13). Check for positive voltage at TP3. If not present, check capacitor C4, resistor R17, and diode CR5; replace defective components. If positive voltage not present at TP3, check 5-second delay transistor Q8 circuit components; replace defective parts. Check for ground at TP5. If not present, troubleshoot amplifier IN-3 (para 6-7*a*).
14	ALARM indicator lamp does not light when alarm condition exists.	*a.* Defective OR gate GOB-1 on assembly A12 (fig. 8-17).	*a*. Troubleshoot OR gate (par a 6-6*d*); replace defective components (fig. 6-13).
		b. Defective amplifier IN-5 (fig. 8-17)	*b*. Troubleshoot amplifier (para 6-7*a*); replace defective components (fig. 6-13).
15	Send data is not transmitted by MD-674(P)/G; no alarms are activated.	*a*. Defective output amplifier Q1, Q2, Q3 on assembly A6 (fig. 8-11).	*a.* Troubleshoot amplifier (see 12*e*(6) above).
		b. Defective output transformer T2 (fig. 6-29).	*b*. Check transformer voltages and resistances (fig. 6-42); replace, if defective.
		c. Defective OUTPUT switch S7.	*c*. Check continuity of switch; replace, if defective (fig. 8-28).
		d. Defective diode CR12 or CR13 on assembly A6 (fig. 8-11).	*d.* Check diodes (fig. 6-7); replace defective components.
16	Receive data not available at output of MD-674(P)/G; no bit-timing signals available for either type of clock oscillator operation.	*a*. Defective 128 divider-A countdown Check module (fig. 8-7).	*a*. for output at pin F of PC 80034100 (fig. 6-3). If not present, check amplifier IN-21 (para 6-7*a*). If present, check for output square wave at test jack J2, if not present, troubleshoot countdown chain (FFC-16 through FFC-22, para 6-5).
		b. Defective BAUD RATE switch S2-. Check	*b*. switch; replace, if defective (fig. 8-28).
		c. Defective countdown circuit on VCO module assembly A1 (fig. 8-6).	*c*. Check for output square wave at test jack J2 on PC 80034090 (fig. 6-2). If not present, troubleshoot countdown circuit (FFC-10, FFC-11, FFC-12, para 6-5); replace defective components.
		d. Defective amplifier IN-15 on assembly A1 (fig. 8-6).	*d*. Troubleshoot amplifier (para 6-7*a*); replace defective components (fig. 6-3).

c. Troubleshooting Chart-Continued

Item No.	Symptom	Probable trouble	Corrective measure
17	No receive data or bit-timing signals available for external clock operation; internal clock operation is normal.	a. Defective amplifier DIA-2 on assembly A1 (fig. 8-6).	a. Take voltage and resistance measurements of Q1-Q5 circuitry (fig. 6-31); replace defective components (fig. 6-2).
		b. Defective OR gate GOA-4 or GOA-5 on assembly A1.	b. Troubleshoot OR gate (para 6-6*d*); replace defective components (fig. 6-2).
		c. Defective AND gate GAI-4 on assembly A1.	c. Troubleshoot AND gate (para 6-6*a*); replace defective components (fig. 6-2).
		d. Defective VCO Q7-Q9 on assembly A1.	d. Check for sine wave output at TP6 of PC 80034090 (fig. 6-2). If not present, check voltage and resistance of VCO (fig. 6-31); replace defective components.
		e. Defective amplifier IN-14 on assembly A1.	c. Troubleshoot amplifier (para 6-7*a*); replace defective components.
18	No receive data or bit-timing data available for internal clock operation; external clock operation is normal.	a. Defective 1.2288 mc crystal oscillator assembly (fig. 1-6).	a. Replace crystal oscillator assembly.
		b. Defective clock module divider FFC-13, FFC-14, or FFC-15 (fig. 8-27).	b. Check for square wave output at test jack J2 (fig. 6-26). If not present, troubleshoot countdown circuit on assembly A33A2 (para 6-5); replace defective parts.
		c. Defective amplifier IN-21 or IN-22 on PC assembly A33A2 (fig. 8-27).	c. Troubleshoot amplifier (para 6-7*a*); replace defective components (fig. 6-26).
19	No receive data or receive bit-timing signals available; uncorrected transmit bit-timing signals normal.	a. Defective add-subtract logic circuit on assembly A3 (fig. 8-8): (1) Defective amplifier IN-24.	a. Troubleshoot add-subtract circuit, as follows: (1) Check for timing signal output at pin U of assembly A3 connector (fig. 6-4). If not present, troubleshoot amplifier IN-24 (para 6-7*a*).
		(2) Defective countdown chain FFD-1, FFD-2, or FFD-3.	(2) Troubleshoot countdown chain (para 6-5); replace defective parts.
		b. Defective 128 divider-B assembly circuit on assembly A4 (fig. 8-9): (1) Defective AND gate GAD-4 or GAD-5. (2) Defective bistable FFG-1. (3) Defective AND gates GAS-6 through GAS-9. (4) Defective countdown chain FFD-5, FFC-23 through FFC-27.	b. Troubleshoot divider-A as follows: (1) Check AND gate (para 6-6*c*); replace defective components (fig. 6-5). (2) Check bistable (para 6-5); replace defective components (fig. 6-5). (3) Check AND gates (para 6-6*c*); replace defective components (fig. 6-5). (4) Check countdown chain (para 6-5); replace defective components (fig. 6-5).

c. Troubleshooting Chart-Continued

Item No.	Symptom	Probable e	Corrective measure
20	No receive data available, but all timing signals are normal; receive carrier alarm not activated, no-transition receive alarm activated.	a. Defective circuit on demodulator module assembly A8 (fig. 8-13):	a. Troubleshoot demodulator as follows:
		(1) Defective amplifier AM-5, AM-6, or AM-8.	(1) Check amplifier in which no output appears (para 6-7*b*); replace defective components (fig. 6-9).
		(2) Defective receive discriminator FL3 or amplifier AM-7.	(2) Check output signal at pin L of PC 80034020 (fig. 6-9). If not present, replace receive discriminator (fig. 2-6) on MX-73(*)/G. If present, check for output at TP2 of PC 80034020 (fig. 6-9); if not present, check amplifier AM-7 (para 6-7*b*).
		(3) Defective operational amplifier Q5, Q6.	(3) Check for output waveform at collector of transistors Q5 and Q6 (fig. 6-9). If not present, make voltage and resistance measurements of applicable operational amplifier (fig. 6-35); replace defective components (fig. 6-9).
		(4) Defective feedback circuit QS or sine Q15.	(4) Check for a wave output at junction of diodes CR2 and CR4 (fig. 6-9); and diodes CR11and CR13. If not present. take voltage and resistance measurements of applicable feedback circuit (fig. 6-35); replace defective components (fig. 6-9).
		(5) Defective shaper circuit Q6 or Q16.	(5) Check for output square wave at TP1 and TP2 of PC 80034020 (fig. 6-9); if not present, take voltage and resistance measurements of the applicable shaper circuit (fig. 6-35).
		(6) Defective phase detector circuit Q7, QS.	(6) Check for output data signal at pin K of PC 80034020 connector (fig. 6-9). If not present, take voltage and resistance of phase detector circuit (fig. 6-35); replace defective components (fig. 6-9).
		(7) Defective amplifier NA-1 .	(7) Take voltage and resistance measurements of Q17, Q18 circuitry (fig. 6-35); replace defective components (fig. 6-9).
		(8) Defective -volt clamp circuit Q19.	(8) Check for output data signal at test jack J2 on PC 80034020 (fig. 6-9). If not present, check amplifier stage Q19 circuitry (fig. 6-35); replace defective components (fig. 6-9).
		b. Defective receive discriminator FL3 on MX-73(*)/G (fig. 2-6).	b. Check for output data signal at TP10 on the control bracket (fig. 2-3); if not present, replace FL3.

c. Troubleshooting Chart-Continued

Item No.	Symptom	Probable trouble	Corrective measure
		c. Defective receive data output module assembly All (fig. 8-16):	c. Troubleshoot receive data output module as follows:
		(1) Defective AND gate GAI-3-	(1) Check AND gate (para 6-6*a*); replace defective components (fig. 6-12).
		(2) Defective AND gate GAD-4 -	(2) Check AND gate (para 6-6*c*); replace defective components.
		(3) Defective amplifier IN-12	(3) Check amplifier (para 6-7*a*); replace defective components.
		(4) Defective bistable FFA-1	(4) Check bistable (para 6-5); replace defective components.
		(5) Defective AND gate GAS-4-	(5) Check AND gate (para 6-6*b*);a replace defective components.
		(6) Defective AND gate GAD-2 -.	(6) Check AND gate (par 6-6*c*); replace defective components.
		(7) Defective risetime and falltime shaper.	(7) Check for output data signal at TP6 of PC 80034030; if not present, check resistors R6 and R7 and transistor Q1. Check for data output signals at TP7; if not present, check resistor R9, capacitor C8, and transistors Q2 and Q7. Check for output data signals at test jack J3 on PC 80034030; if not present, check resistors R10 through R16, diodes CR6, CR8, and C R9, and transistors Q3, Q8, and Q9. Replace defective components.
		(8) Defective amplifier POD-1	(8) Check for output data signal at test jack J3 on PC 80034030. If not present, check amplifiers Q3, Q8, Q9 circuitry (fig. 6-38); replace defective components.
		d. Defective ORDER WIRE RECEIVE jack J2.	d. Check jack; replace, if defective (fig. 8-28).
		e. Defective feedthrough capacitor C20 or C21 (fig. 6-29).	e. Check capacitors; replace, if defective (fig. 6-29).
21	Receive carrier alarm not activated when receive input data is removed.	a. Defective third input amplifierQ15 on assembly A9 (fig. 8-14) or defective resistor A8R2 on assembly A8 (fig. 6-9).	a. Troubleshoot third input amplifier as follows:
		(1) Defective resistor A8R2	(1) Check for ground or slight positive voltage at test jack J3 on PC assembly A8 (fig. 6-9). If not present, check resistor A8R2; replace resistor, if defective.
		(2) Defective third input amplifier Q15.	(2) Check for a negative voltage at TP2 of PC 80034050 (fig. 6-10). If not present, take voltage and resistance measurements of transistors Q3 through Q6 and Q15; replace defective components.

c. Troubleshooting Chart-Continued

Item No.	Symptom	Probable trouble	Corrective measure
21	Receive carrier alarm not activated when receive input data is removed-Con.	b. Defective level threshold circuit Q3-Q6.	b. Check REC CARRIER ALARM THRESHOLD resistor 1A1R11 (fig. 8-28); make voltage and resistance measurements of Q3-Q6 (fig. 6-36); replace defective components (fig. 6-10).
		c. Defective amplitude detector circuit Q7, Q8, Q9.	c. Check for negative voltage at TP3 (fig. 6-10). If not present, take voltage and resistance measurements of transistors Q7, Q8, and Q9; (fig. 6-36) replace defective components (fig. 6-10).
		d. Defective amplifier IN-10 .	d. Check for - 15 volts at the junction of diodes CR7 and CR8 on PC 80034050 (fig. 6-10); if not present, check amplifier IN-10 (para 6-6*a*).
		e. Defective OR gate GOC-1 defective components (fig. 6-10).	e. Check OR gate (para -6*d*); replace
		f. Defective amplifier IN-9	f. Check amplifier (para 6-7*a*); replace defective components (fig. 6-10).
		g. Defective 2-econd delay circuit Q11, Q12.	g. Check for ground at TP4 on PC 80034050 (fig. 6-10). If not present, check transistor Q11, capacitor C9, diode CR4, and resistor R34 (fig. 6-10); replace defective components. If present, check for +6 volts at test, jack J4 on PC 80034050; if not present, check transistor Q12 circuitry (fig. 6-10) and replace defective components.
22	No receive data output available; receive carrier alarm and no-transition receive alarm are activated; all bit-timing signals are normal.	a. Defective first and second input amplifier Q1, Q2, Q16 on assembly A9 (fig. 8-14).	a. Troubleshoot first and second input amplifier Q1, Q2, Q16 circuitry (fig. 6-36); replace defective components (fig. 6-10).
		b. Defective EQUALIZER switch S1 (if used) (fig. 2-7 or 2-8).	b. Replace switch (if used); replace if defective (fig. 6-44 or 6-45).
		c. Defective receive filter FL1 on MX-73(*)/G (fig. 2-6).	c. Replace receive filter FL1 (fig. 2-6).

c. Troubleshooting Chart-Continued

Item No.	Symptom	Probable trouble	Corrective measure
		d. Defective equalizer circuit on assembly A235A (if used) (fig. -25).	*d*. Check for input fsk signal at pins N and G of PC 80034230 (fig. 6-25); if not present, take voltage and resistance measurements of Q1 circuitry (fig. 6-41), and replace defective components. Check for fsk signal at pins U and V of PC 80034230 (fig. 6-25); if not present, take voltage and resistance measurements of Q2-Q3 circuitry (fig. 6-41), and replace defective components. Check for fsk signal at test jack J2 on assembly A25A3 (fig. 6-25); if not present, take voltage and resistance measurements of Q4 circuitry (fig. 6-41), and replace defective components.
23	Improper operation when order-wire circuit operation is initiated.	a. Defective talk generator circuit (fig. 8-8): (1) Defective amplifier IN-25 on PC 80034140. (2) Defective OR gate GOA-6 (3) Defective bistable FFE-1 or FFF-1. (4) Defective 1.5-second delay circuit QS, QG, Q7.	a. Troubleshoot talk generator circuit as follows: (1) Check amplifier (para 6-7*a*); replace defective components (fig. 6-4). (2) Check OR gate (para 6-6*d*); replace defective components. (3) Check bistable (para 6-5); replace defective components. (4) Check for - 15 volts at TP4 of PC 80034140 (fig. 6-4); if not present for approximately 1.5 second after talk-request is initiated (signal returns to ground after 1.5 second), take voltage and resistance measurements of 1.5-second delay (Q5, Q6, Q7 circuitry, fig. 6-32). Replace defective components.

c. Troubleshooting Chart-Continued

Item No.	Symptom	Probable trouble	Corrective measure
24	Improper operation when order-wire talk-request signal is received.	a. Defective talk-request detector module:	a. Troubleshoot talk-request detector module as follows:
		(1) Defective amplifier IN-16 on assembly A10 (fig. 8-15).	(1) Check amplifier (para 6-7*a*); replace defective components (fig. 6-11).
		(2) Defective initial timer Q2, Q3, Q4.	(2) Check for +6 volts at the collector of transistor Q4 on PC 80034040 (fig. 6-11) at the time of talk-request generation. If not present, take voltage and resistance measurements of the initial timer (Q2, Q3, and Q4 circuitry, fig. 6-37); replace defective components.
		(3) Defective window timer Q5, Q6, Q7.	(3) Check for +-6 volts at the collector of transistor Q7 on PC 80034040 (fig. 6-11), approximately 1 second after the talk-request is generated, then check for a ground approximately 3/4 of a second later. If the voltage indications are not correct, take voltage and resistance measurements of the window timer (Q5, Q6, and Q7) circuitry, fig. 6-37); replace defective components.
		(4) Defective amplifier IN-17	(4) Check amplifier (para 6-7*a*); replace defective components.
		(5) Defective AND gate GAD-3	(5) Check AND gate (para 6-6*c*); replace defective components.
		(6) Defective amplifier IN-18	(6) Check amplifier (para 6-7*a*); replace defective components.
		(7) Defective bistable FFB-1	(7) Check bistable (para 6-5); replace defective components.
		(8) Defective amplifier IN-19 or IN-20.	(8) Check amplifier (para 6-7*a*); replace defective components.
		(9) Defective OR gate GOE-1	(9) Check OR gate (para 6-6*d*); replace defective components.
		(10) Defective AND gate GAS-5	(10) Check AND gate (para 6-6*b*); replace defective components.
25	Order-wire circuit cannot be reset when TALK REQUEST RESET push-button is depressed.	a. Defective TALK REQUEST RESET switch S4.	a. Check switch; replace, if defective (fig. 8-28).
		b. Defective feedthrough capacitor C12 (fig. 6-29).	b. Check capacitor; replace, if defective (fig. 6-29).
26	No transmit bit-timing signals available.	a. Defective risetime and falltime shaper No. 2 on assembly A5 (fig. 8-10).	a. Check for bit-timing signals at TP3 of PC 80034150 (fig. 6-6). If not present, take voltage and resistance measurements of shaper No. 2 (Q1, Q2, Q3, Q4 circuitry, fig. -33); replace defective components (fig. 6-6).

c. Troubleshooting Chart Continued

Item No.	Symptom	Probable trouble	Corrective measure
26		*b*. Defective amplifier PDA-3 or PDA-4 on assembly A5 (fig. 8-10).	*b*. Check for bit-timing signals at test jacks J2 and J3 on PC 80034150 (fig. 6-6). If not present at J2, take voltage and resistance measurements PDA-3 (Q5 and Q6 circuitry, fig. 6-33), and replace defective component. If not present at J3, take voltage and resistance measurements of PDA-4 (Q7 and Q8 circuitry, fig. 6-33); replace defective components (fig. 6-6).
27	No receive bit-timing signals available.	*a*. Defective risetime and falltime shaper No. 1 on assembly A5 (fig. 8-10).	*a*. Check for bit-timing signals at TP6 of PC 80034150 (fig. 6-6). If not present, take voltage and resistance measurements of shaper No. 1 (Q9, Q10, Ql11 Q12 circuitry, fig. 6-33); replace defective components (fig. 6-6).
		b. Defective amplifier PDA-1 or PDA-2 on assembly A5 (fig. 810).	*b*. Check for bit-timing signals at test jacks J5 and J6 on PC 80034150 (fig. 66). If not present at J5, take voltage and resistance measurements orf PDA-2 (Q15 and Q16 circuitry, fig. 6-33); replace detective components (fig. 6-6).
28	No external common alarm available or no synchronizer, disable output.	Defective amplifier IN-6 on assembly A12(fig. 811).	Troubleshoot amplifier (para 6-7a); replace defective components (fig. 6-7).

6-5. Isolating Troubles in Multivibrator Stages

Every bistable multivibrator stage used in the equipment is essentially the same, only the input triggering method is different; therefore, only the bistable multivibrator stage shown in B, figure 5-1, is described below in detail. To check the other configurations of the bistable multivibrator stages, follow the same procedures and check the transistors and input steering diodes. Refer to the appropriate schematic diagram for specific reference designations and component values. Before checking any bistable multivibrator stage, disconnect all signals by removing appropriate PC assemblies (refer to the logic diagram (fig. 8-5) for specific PC assemblies to be removed), and turn on the power. When several bistables are used in a countdown chain. ascertain which bistable is defective by checking for an output square wave from the first bistable to the last. The first bistable that has no output is probably defective.

a. Connect the ME-26A/U (set to measure - 30 volts dc) between the collector of transistor Qa and ground.

b. Momentarily short the transistor Qa base to emitter. If the collector voltage observed in a above is 0 volt, the ME-26A/U should indicate approximately -6 volts. If the voltage observed in (i above is not -6 volts, check for open resistor Ra, open diode CRa, or shorted resistor Rc.

c. Connect the ME-26A/U between the collector of transistor Qb and ground.

d. Check the transistor circuit as described in b above. If the voltage observed is not -6 volts, check for open resistor Rb, open diode CRb, or shorted resistor Rd.

c. Cut off transistor Qa by momentarily shorting its base to emitter, and check the voltage at the collector of transistor Qb. The voltage indication should be approximately 0 volt. If not, check for open resistor Rc or Re or defective transistor Qb.

f. Cut off transistor Qb by momentarily shorting its base to emitter, and check the voltage at the collector of transistor Qa. The voltage indication should be approximately 0 volt. If not, check for open resistor Rd or Rf or defective transistor Qa.

g. If proper results are obtained in *b* through *f* above, check the steering circuit by removing power from the unit and checking the forward resistalnce of diodes CRc and CRd (the resistance measured should be in the order from 1 to 10 ohms). Check for defective input capacitor Ca or C11, or defective steering resistor Rg or Rh.

6-6. Isolating Troubles in Logic Gates

(figs. 5-5 and 5-6)

Troubleshooting procedures for each type of logic gate are given below. Refer to the appropriate schematic diagrams for specific reference designations and component values. All procedures are performed with the applicable PC card extended and with power applied.

a. *Inverting AND Gate (GAI-( ) Type*).

The AND gates shown in C and D, figure 5-5, operate essentially the same. The main difference is that the AND gate shown in C requires two positive inputs to be enabled, and the AND gate shown in D requires two negative inputs to be enabled.

Check the gates as follows:

(1) Jumper the input side of each input element to a source of - 15 volts de. (Refer to the applicable schematic diagram and PC card layout for this voltage point.)

(2) Check the voltage at the collector of the transistor. The voltage indication should be approximately zero for the AND gate shown in C, and approximately -15 for the AND gate shown in D. If not, check for open collector load resistor, defective base return resistor or diode, or open transistor. (For the type shown in C, figure 5-5, also check for open base limiting resistor Ra.)

(3) Remove the jumper to the -15-volt source and jumper the input side of each input element to ground. The voltage at the collector of the transistor should indicate approximately -15 volts de for the AND gate shown in C and 0 volt for the AND gate shown in D. If not, check for shorted collector load resistor, shorted base return resistor or diode, or shorted transistor.

(4) Remove the jumper from each input resistor in turn, returning the input resistor to the -15-volt source. With any input element of the AND gate shown in C returned to - 15 volts de, the collector voltage of the transistor should indicate approximately 0 volt; with any input element of the AND gate shown in D returned to ground, the collector voltage of the transistor should indicate approximately 0 volt. If not, check for an open input element.

b. AND Gate, GAS-( ) Type (B, fig. 5-5).

(1) Connect the ME-26A/U between the output of the gate and ground.

(2) Jumper the input side of resistor Ra to a -15-volt source. (Refer to the applicable schematic diagram and PC card layout for this voltage point.)

(3) Alternately jumper the input side of capacitor Ca to -15-volt source and then to ground. The ME-26A/U should indicate 0 volt at all times. If not, check for open resistor Ra or shorted diode CRa.

(4) Jumper the input side of resistor Ra to ground, and alternately jumper the input side of capacitor Ca to -15-volt source. The ME-26A/UI should indicate some negative value when the input is negative, and 0 volt when the input is ground. If not, check for open capacitor Ca or open diode CRa.

c. AND Gate, GAD-( ) Type (A, fig. 5-5).

(1) Jumper the input side of each diode to a - 15-volt source (refer to the applicable schematic diagram and PC card layout), and check the voltage between the output of the gate and ground. The voltage indication should be a negative potential of less than - 15 volts. If not, check for open resistor Ra, open resistor Rb, or shorted diode CRa or CRb.

(2) Remove the -15 volts from diode CRa, and jumper CRa to ground. (Refer to the appropriate schematic diagram and PC card layout for this point.) The ME26A/U should indicate approximately 0 volt. If not, check for open diode CRa or shorted resistor Rb.

(3) Reconnect the input side of diode CRa to a - 15-volt source; remove diode CRb from the -15-volt source, and connect it to ground. The ME-26A/U should indicate approximately 0 volt. If not, check for open diode CRb.

d. *OR Gates*. The OR gates shown in figure 5-6 operate essentially the same way with a positive input applied to any input to enable the gate. Check the GOA- and GOB-type OR gates as described in (1) below-; check the GOa- and Gob-type OR gates as described in (2) below.

(1) GOA- and GOB-type OR gates.

(a) Connect the input side of all input elements (illustrated by diodes CRa and CRb in A, fig. 5-6) to a source of - 15 volts de. (Refer to the applicable schematic diagram and PC card layout for this voltage point.)

(b) Check the voltage across resistor Rc.

The voltage indication should be approximately 0 volt. If not, check for open resistor Rc or shorted diode CRa or CRb.

(c) Remove the - 15 volts from the input of CRa, and jumper the input to ground. The voltage across resistor Ra should indicate approximately 0 volt; if not, check for open diode CRa, open resistor Ra, or shorted resistor Re.

(d) Return the input side of diode CRa to - 15 volts, and jumper the input side of diode CRb to ground. The voltage indication should be approximately 0 volt. If not, check for open diode CRb or0 open resistor Rb.

(2) GOC- and GOE-type OR gates.

(a) Connect the input side of diodes CRa and CRb to a source of -15 volts dc. Refer to the applicable schematic diagram and PC card layout for this voltage point.

(b) Check the voltage between the output and ground. The voltage indication should be approximately 0 volt. If not, check for shorted diode CRa and resistor Ra or diode CRb.

(c) If the voltage indications in (*b*) above are correct, check for open circuit elements.

6-7. Isolating Troubles in Amplifier Stages

a. Inverting Amplifier (A, fig. 5-7).

(1) Jumper the input side of resistor Ra, to ground, and monitor the collector voltage of transistor Qa (ME-26A/U set to measure - 30 volts dc).

(2) The voltage at the collector of transistor Qa should be approximately -6 volts. If not, check for a shorted transistor, open resistor Pb, or open diode CRa (if used).

(3) Remove the ground connection from resistor Ra., and jumper the input side of resistor Ra to a -15-volt source. (Refer to the applicable schematic diagram and PC card layout for this point.)

(4) The voltage at the collector of transistor Qa should be approximately 0 volt. If not, check for open resistor Ra, shorted resistor Rb or Rc, shorted diode CRa or CRb (if used), or open transistor.

b. Noninverting Amplifier (Emitter Follower) (B, fig. 5-7). Two types of emitter-follower circuits are used in the equipment, one employing a PNP transistor ((1) below), and the other employing a NPN transistor with a collector limiting resistor ((2) below).

(1) PNP emitter follower.

(a) Jumper the base of transistor Qa, to ground, and monitor the emitter voltage of transistor Qa (ME-26A/U set to measure - 30 volts dc).

(b) The voltage at the emitter of transistor Qa should be approximately 0 volt. If not, check for shorted transistor Qa.

(c) Remove the ground connection from the base of the transistor, and jumper the base to a -15-volt source. (Refer to the applicable schematic diagram and PC card layout for this point.)

(d) The voltage at the emitter of the transistor should be approximately -15

volts. If not, check for defective resistoIr Ra or open transistor Qa.

(2) NPN emitter follower.

(a) Jumper the input side of resistor Ra to ground, and monitor the emitter voltage of transistor Qa (ME-26A/U set to measure -30 volts dc).

(b) The voltage at the emitter of transistor Qa should be approximately 0 volt. If not, check for shorted transistor Qa.

(c) Remove the ground from resistor Ra, and connect it to a +15-volt source.

(Refer to the applicable schematic diagram and PC card layout for this voltage point.)

(d) The voltage at the emitter of the transistor should be a positive voltage of less than + 15 volts. If the voltage indication is 0 volt, check for open resistor Ra or Re, shorted resistor Re or Rd, or open transistor Qa. If the voltage is +15 volts, check for shorted resistor Ra.

6-8. Repair Procedures

a. Front Panel Components. To reach the rear of the front panel controls and indicators, proceed as follows:

(1) Remove the knob from the BAUD RATE switch (fig. 3-1), and disengage the switch from the front panel by removing the hexagonal securing unit.

(2) Remove the front panel screws that secure the ferrous metal shield (fig. 1-6) over the front panel components; move the shield away from the front panel.

Caution: Be careful, when removing the shield, not to damage the plastic shaft to the BAUD RATE switch and to the OUTPUT LEVEL ADJ control, or the wiring to the feedthrough capacitors mounted on the shield.

(3) With the metal shield disengaged from the front panel, all controls and indicator connection points, as well as both sides of the feedthrouglh capacitors, are accessible.

(4) To replace the shield, slide the plastic shaft over the switch and resistor control shafts; work the shafts through the holes in the front panel. Secure the BAUD RATE switch to the front panel with the securing nut, and replace the knob on the switch shaft. Secure the shield to the front panel with the front panel screws. Be sure that all screws are tightened.

b. Power Supply Submodule Repairs (fig. 6-18

Note. Before removing any component, tag its connecting wires to be sure that they are replaced properly.

(1) To remove any of diodes CR1 through CR5, remove the mounting nut that secures the diode to its mounting plate. Push the diode through the mounting plate, and unsolder the connecting wires.

(2) To remove a transistor, the heat sink assembly must be disassembled as follows:

(a) Remove the four heat sink mounting screws.

(b) Separate the heat sink assembly from the chassis, so that the transistor connecting leads are accessible.

(c) Unsolder the connecting wires, and remove the transistor from the heat sink by removing the transistor securing screws.

(3) To remove fan motor assembly B1, remove the fan mounting screws that secure the fan assembly to the frame. Unsolder the motor leads from connector P1, and remove the fan assembly.

(4) To replace any component of the power supply submodule, reverse the applicable procedures given in (1), (2), and (3) above.

c. Crystal Oscillator and Oven Assembly (fig. 6-21).

Note. Before removing any component, tag the connecting wires to be sure that they are replaced properly.

(1) Remove the receive and transmit filters (fig. 2-7) by removing the mounting nuts that secure each filter to the MX-73(*)/G. Pull each filter straight up and remove it.

(2) Remove the cover from the crystal oscillator and oven assembly, by unscrewing the screws that secure the cover to the MX-73(*)/G and pulling the cover straight up and out. Remove the insulating material

from around the crystal oscillator and oven assembly, noting the installation to to be sure it is replaced in the same relative position.

(3) Remove the top of the crystal oscillator and oven assembly by unscrewing the screws on each side of the can. Transistor 1A1Q1 is mounted to this cover; be careful of the wire connections between the transistor and the PC assembly.

(4) To remove the PC assemblies in the crystal oscillator and oven assembly, unscrew the screws that secure each PC assembly to the side of the can. The two lower screws for each PC assembly are removed through the access holes in the MX-73(*)/G chassis. PC 80034212 can now be removed from the can.

(5) To remove PC 80034220, remove the tape that secures the excess lead wire to the can. While pulling the PC assembly up and out of the can, feed the cable through the bottom.

(6) To reassemble the crystal oscillator and oven assembly, reverse the procedures given in (1) through (5) above.

d. Printed-Circuit Card Repairs. Refer to TB SIG 222 to replace parts on printed-circuit cards.

CHAPTER 7

GENERAL SUPPORT TESTING PROCEDURES

7-1. General

a. These testing procedures are prepared for use by Electronic Field Maintenance Shops and Service Organizations responsible for general support maintenance of electronic equipment to determine the acceptability of repaired electronic equipment. These procedures set forth specific requirements that repaired electronic equipment must meet before it is returned to the using organization. A summary of the performance standards is given in paragraph 7-9.

b. Each test depends on the preceding one for certain operating procedures and, where applicable, for test equipment calibration. Comply with the instructions preceding the body of each chart before proceeding to the chart. Perform each test in sequence. Do not vary the sequence. For each step, perform all actions required in the Control settings column; then perform each specific test procedure and verify it against its performance standard.

7-2. Test Equipment and Material Required

All test equipment, materials, and other equipment required to perform the testing procedures given in this section are listed in a and b below and are authorized under TA 11-17 and TA 11-100 (11-17), TOE 11-158E and TA 11-101 (11-158) or are repair part items of subject equipment authorized for storage at general support facilities. Specific models and types of test equipment were used to perform the general support test procedures. If these testing procedures are performed with other models or types of the test equipment, an allowance must be made for any test connections or test result that may differ from those given in these test procedures.

a. Test Equipment.

See Maintenance Allocation Chart Section III for test equipment

b. Material.

Item	Federal stock No.
Plug PL55, 4 each----------	5935-201-7951
Hookup wire, #18 AWG (as required) ---	6145-160-5317
Clips, alligator (as required)----------	5940-186-8933
11-pin female socket, Amphenol Type 78811M.	5935-240-0456

7-3. Test Facilities

a. Ac Power. All tests should be performed with the use of 115 to 120 volts, 60 cycles per second. All connecting cables are part of the test equipment or equipment under test, unless otherwise indicated on the applicable illustrations.

b. Test Cable Assemblies.

(1) *Data cable*. Fabricate two data test cables as follows:

(a) Connect a 4-foot length of wire between the tips of two Plugs PL-55.

(b) Connect a second 4-foot length of wire between the sleeves of each PL55.

(2) Line Amplifier LA-1 test cable. Solder 4-foot lengths of hookup wire to pins 1, 2, 3, 4, 9, and 10 of the 11-pin female socket.

7-4. Modification Work Orders

The performance standards in the tests (paras 7-5 through 7-8) assume that no modification work orders (MWO's) have been performed on the equipment. A listing of current modification work orders may be found in DA Pam 310-74. If a modification work order is performed on the equipment, an allowance must be made for any test connections or test results that may differ from those given in these test procedures.

7-5. Physical Tests and Inspection

a. Test Equipment and Materials. None.
b. Test Connections and Conditions.
(1) No connections are required.
(2) The following tests are performed with the MD-674(P)/G extended from its ferrous metal case.
c. Procedures.

Step	Control settings		Procedure	Performance standard
	Test equipment	Equipment under test		
1	N/A	Controls may be in any position.	*a*. Inspect front panel. Look for damaged, loose, or missing screws, knobs, or other parts.	*a*. No evidence of damages, loose or missing screws, knobs, or parts is found.
			b. Inspect front panel and chassis (top and bottom). Look for cleanliness, signs of excessive wear or damage, loose or missing components and hardware.	*b*. Front panel and chassis are clean. No evidence of excessive wear, damage, or loose components or hardware are found.
			c. Inspect condition of finish. Look for rust, corrosion, and spots where bare metal is exposed. *Note*. Touchup painting is recommended instead of refinishing. Screwheads and receptacles will not be polished with brushes.	*c*. External surfaces intended to be painted do not show bare metal. Panel lettering is legible.
			d. Operate each switch and control on front panel and control bracket. Look for smooth and positive operation.	*d*. Switches and controls operate smoothly with positive action to indicated positions.
			e. Inspect condition of jacks and lamps. Look for cracks, broken parts, and condition of jack spring contacts. closing.	*e*. No evidence of cracks or broken parts. Jack contact springs are straight and show positive action in opening and
			f. Inspect chassis; be sure PC cards are in proper places.	*f*. PC cards are in proper places and firmly seated.
2	N/A	Controls may be in any. position.	Check equipment for applicable modification work order (see DA Pam 310-4 for list of MWO's).	If MWO is performed, MWO number appears on equipment.

7-6. Data Test

(fig. 7-1)

a. Test Equipment and .Material.

See Maintenance Allocation Chart Section III for test equipment.

b. Test Connections and Conditions.

(1) Remove the test MD-4(P)/G from its case and install the repaired MD-674(P)/G in its place, or remove the appropriate plug-in module from the test MD-474(P)/G, and install the repaired plug-in module in its place
(2) Connect the equipment as shown in A and B, figure 7-1.
(3) Adjust DD-205A controls to obtain test pattern on screen.
(4) Strap together only terminals 5 and 6, on the bottom of the harness card.
(5) Strap together terminals 1, 2, and 3, on PC a ,assembly AS.
(6) Strap together terminals 2 and 4 on PC assembly All.
(7) Operate all POWER switches to the on position.

c. Procedure.

Step No.	Control settings		Procedure	Performance standard
	Test equipment	Equipment under test		
1	PG-205A CHARACTER RELEASE: FREE RUN. DISTORTION: OFF. 37.5 EXTERNAL: -1200 PATTERN SELECTOR: REVERSALS. BAUDS: As required. JACK SIGNAL SELECTOR: LOW LEVEL.	BAUD RATE: As required. ALARM: DISABLE. INPUT: 600Ω. OUTPUT: 600Ω. INPUT SELECT: DATA.	a. Rotate OUTPUT LEVEL ADJ control from one extreme to the other. b. Adjust OUTPUT LEVEL ADJ control for 0 dbm on ME-30A/U, or equivalent. c. Operate INPUT SELECT switch to MARK.	*a.* ME-30A/U should indicate between -20 dbm and +3 dbm; DD-205A SIGNAL lamp should light and meter should indicate less than 3.5% distortion (2% for MX-7379/G). *b.* None. *c.* Electronic Counter 5233L should indicate as follows for each MX-73(*)/G (±0.5 cps): MX-7372/G: 425 cps.

c. Procedure- Continued

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Procedure	Performance standard
1	*DD-205A* TRANSITION SELECT: SPACE Left hand: ALL MARK Right, hand: ALL,. DISTORTION SELECT: AVG. INPUT FILTER: OUT. EXTERNAL: 37.5 1200 INPUT POLARITY: As required. INPUT SELECT: POLAR LOW LEVEL BAUDS: As required. Toggle switch: SYNCHRONOUS. RESET: AUTO. *350D* DB: 0. *Electronic Counter 5tSSL* FUNCTION: FREQUENCY A. TIME-BASE-MULTIPLIER: luS10^{6}. SAMPLE RATE: Midposition. COM-SEP-CHECK: SEP. DC VOLTS-AC VOLTS: AC VOLTS X 100. *ME-86A/U* SELECTOR: DC. RANGE: 10V.		*d*. Operate INPUT SELECT switch to SPACE.	MX-7373/G: 510 cps. MX-7374/G: 765 cps. MX-7375/G: 680 cps. MX-7376/G: 1105 cps. MX-7377/G: 1190 cps. MX-7378/G: 1445 cps. MX-7379/G: 1200 cps. MX-7380/G: 1785 cps. MX-7381/G: 1870 cps. MX-7382/G: 2125 cps. MX-7383/G: 2040 cpa. MX-7384/G: 2465 cps. MX-7385/G: 2550 cps. MX-7386/G: 2805 cps. *d*. Electronic Counter 5233L should indicate as follows for each MX-73 (*) /G (±0.5 cps): MX-7372/G: 595 cps. MX-7373/G: 850 cps. MX-7374/G: 935 cpa. MX-7375/G: 1360 cps. MX-7376/G: 1275 cps. MX-7377/G: 1530 cps. MX-7378/G: 1615 cps. MX-7379/G: 2400 cps. MX-7380/G: 1955 cps. MX-7381/G: 2210 cps.

	ME-30A/U Range selector: -20 DB.			MX-7382/G: 2295 cps. MX-7383/G: 2720 cps. MX-7384/G: 2635 cps. MX-7385/G: 2890 cps. MX-7386/G: 2975 cps.
			e. Operate INPUT SELECT switch to OFF.	*e*. Electronic Counter 5233L should not indicate any output frequency; SIGNAL lamp on DD-205A should light. Meter should indicate maximum distortion.
2	No change required.....	.....	a. Operate INPUT SELECT switch to DATA.	*a*. Reversals pattern should be observed on DSS-205A scope. Signal amplitude shall be 12 volts ±2.
			b. Set Attenuator 350D for -35 dbm indication on ME-30A/U.	*b*. DD-205A should indicate not more than 8% distortion for all units, except MX-7379/G, which should indicate not more than 2%.
			c. Set DD-205A DISTORTION SELECT switch to TOTAL PEAK.	*c*. DD-205A should indicate not more than 8% distortion for all units, except MX-7379/G, which should indicate not more than 5%.
3	No change required, except: *Power Supply T-50-2* VOLTMETER RANGE: 50 VOLTS. METER: VOLTS.	Same as step No. 1, except: OUTPUT LEVEL ADJ control: Fully clockwise	*Note.* Do not disconnect MhE-26A/U from terminals 3 and 4 of terminal board TB3. a. Connect equipment as shown. in A and C, figure 7-1. b. Operate T-50-2 POWER switch to on position and adjust VOLTAGE ADJUST and VOLTAGE VERNIER for 48 volts.	*a*. None *b*. None.

c. Procedure-Continued

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Procedure	Performance standard
3	No change required-Continued	Same as step No. 1-Con.	c. Adjust GAIN control on the LA-1 for + 7 dbm indication on ME-30A/U.	c. DD-205A should indicate not more than 3.5% distortion for all units, except MX-7379/G, which should indicate not more than 2%; reversals pattern should be evident on DSS-205A.
			d. Set DD-205A DISTORTION SELECT switch to AVG.	d. DD-205A should indicate not more than 3.5% distortion for all units, except MX-7379/G, which should indicate not more than 2%.
4	No change required, except: *PC-205A* DISTORTION SELECT: SPACING BIAS. PER CENT DISTORTION: 10.	Same as step No. 3	a. Observe DD-205A meter.....	a. Meter on DD-205A should indicate not more than 3.5% distortion for all units, except MX-7379/G, which should indicate not more than 2%.
			b. Operate DISTORTION SELECT switch on PG-205A to MARKING BIAS.	b. Meter on DD-205A should indicate not more than 13.5% distortion for all units, except MX-7379/G, which should indicate not more than 12%.
			c. Set DD-205A DISTORTION SELECT switch to TOTAL PEAK.	c. Meter on DD-205A should indicate no more than18% distortion, except MX-7379/G, which should indicate no more than 15%.
			d. Set DD-205A DISTORTION SELECT switch to AVG and depress TALK REQUEST pushbutton.	d. Meter on DD-205A should indicate 10% distortion (±29), for a 1.5-second period, and then return to no more than 13.5% (12% for MX-7379/G); ME-26A/U indication changes from 6.25 vdc to 0 ±5 v; TALK REQUEST indicator lamp on MD-674(P)/G should be lighted.
			e. Depress TALK REQUEST RESET pushbutton.	e. Meter on DD-205A should indicate no more than 13.5% distortion (12% for MX-7379/G); ME-26A/U indication changes from 0 to +6.25v ±5% TALK REQUEST indicator lamp on MD-674(P)/G should be-extinguished.

7-7. Timing Tests

a. Test Equipment and Material.

(1) Test Modem, Low- Speed Wire Line MD-674(P)/G.
(2) Data analysis center, Stelma model DAC-6A.
(3) Electronic counter, Hewlett-Packard model 5233L.
(4) Oscilloscope, Hewlett-Packard model 140A with plug-ins 1405A and 1421A.
(5) Hookup wire.

b. Test Connection and Conditions.

(1) Remove the test MD-674(P)/G from its case, and install the repaired MD-674(P)/G in its place, or remove the appropriate plug-in module from the test MD-674(P)/G, and install the repaired plug-in module in its place.
(2) Install Clock Module Group OA-8072/G (original or repaired) in the MD-674(P)/G.
(3) Connect the equipment as shown in figure 7-2.
(4) Strap, together, terminals TP4 and TP5 on PC assembly A1.
(5) Operate all POWER switches to the on position.

c. Procedure.

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Procedure	Performance standard
1	*PG-205A* BAUDS: As required. Selector switch: SYNCBIT-TIME. PATTERN SELECTOR: REVERSALS. CHARACTER RELEASE: FREE RUN. DISTORTION: OFF. EXTERNAL: 37.5 / 1200 JACK SIGNAL SELECTOR: LOW LEVEL. *Electronic Counter 52331.* FUNCTION: FREQUENCY A. TIMEBASE-MULTIPLIER: 1uS10^{6}. SAMPLE RATE: Midposition. COM-SEP-CHECK: SEP.	BAUD RATE: As required. ALARM: DISABLE. INPUT SELECT: DATA.	a. Observe indication on 5233L. *b.* Remove 5233L connections from terminals 10 and 11, and connect them to terminals 1 and 2. c. Remove 5233L connections from terminals 1 and 2, and connect them to terminals 4 and 5. *d.* Remove 5233L connector from terminals 4 and 5, and connect them to terminals 7 and 8. *e.* Observe both patterns on the 140A oscilloscope. *f.* Remove 140A oscilloscope connections from terminals 1 and 2 (TB2) and connect them to terminals 4 and 5.	a. 5233L should indicate frequency equal to baud rate of equipment under test, ±2%. *b.* 5233L should indicate as in a above. *c.* 5233L should indicate as in a above. *d.* 5233L should indicate as in a above. *e.* Pattern should be of same frequency but not necessarily in synchronism. *f.* Pattern should appear synchronous, with all data (input A) and timing (input B) transitions in alignment.

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Procedure	Performance standard
	DC VOLTS-AC VOLTS: AC VOLTS X 100. then to ON; observing 140A *Oscilloscope 140A, 1405A (both channels* COUPLING: DC. INPUT: ON FUNCTION: A. -POLARITY: +. VERNIER SENSITIVITY: .2. SENS MAG: X1 *1421A* SWEEP: MAIN. MAGNIFIER: X1. NORMAL-SINGLE: NORMAL. DELAYED TIME/CM: OFF.		*g*. Operate AC POWER switch on low seed modem to of and with top waveform.	*g*. Bottom timing waveforn should be seen to move into synchronism
2	No change required.....	No change required, except: AC POWER: off.	*a*. Remove strap from between ter-. minal TP4 and TP5, and connect a strap between terminals TP3 and TP4. *b*. Operate AC POWER switch on MD-674(P)/G to ON.	*a*. None *b*. 5233L shall indicate frequency equal to baud rate of equipment; 140A oscilloscope waveform pattern shall be as observed in step No. 1*f*.

7-8. Alarm Tests

a. Test Equipment and Material.

See Maintenance Allocation Chart Section III for test equipment.

b. Test Connections and Conditions.

(1) Remove the test MD-674(P)/G from its case, and install the repaired MD-674(P)/G in its place, or remove the appropriate plug-in module from the test MD-674(P)/G, and install the repaired plug-in module in its place.

(2) Connect the equipment as shown in A and B of figure 7-3.

(3) Strap, together, terminals TP4 and TP5 on PC assembly A1.

(4) Operate all POWER switches to the ON position.

c. Procedure.

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Procedure	Performance standard
	PG-205A	BAUD RATE: As required. ALARM: NORM.	*a*. Note indication on ME-30A/U	a. ME-30A/U should indicate between +3 dbm and - 20 dbm.
1	CHARACTER RELEASE: FREE RUN DISTORTION: OFF EXTERNAL: 37.5 / 1200 PATTERN SELECTOR: REVERSALS BAUDS: As required JACK SIGNAL SELECTOR: LOW LEVEL (MECH OFF).	INPUT: 600Ω. OUTPUT: 600Ω. INPUT SELECT: DATA.	*b*. Connect ME-26A/U between test point TP8 on control bracket and ground and adjust front panel OUTPUT LEVEL ADJ control slowly until ME-26A/U changes from 13.5: volt indication to -15 volts indication.	*b*. Front panel ALARM indicator lamp should light approximately 2 seconds after ME-26A/U indicates -15 volts.
			c. Make a note of indication on ME-30A/U.	*c*. ML-3A /U should indicate ap-Proximately 10 dbm less than reading in a above.
	DD-205A TRANSITION SELECT: Left hand: -SPACE / MARK Right hand: ALL. DISTORTION SELECT: AVG. INPUT FILTER: OUT EXTERNAL: .37.5 / 1200 INPUT POLARITY: As required. Toggle switch: SYNCHRONOUS.		*d*. Adjust front panel OUTPUT LEVEL ADJ control slowly until ALARM indicator lamp is extinguished; make note of indication on ME-30/U.	d. ME-30 A/U should indicate 5 dbm (±1 dbm) less than indication in *a*. above.

Step No.	Test equipment	Control settings Equipment under test	Procedure	Performance standard
	RESET: AUTO *350D* DB: 0. *ME-.3OA/U* Range selector: -20DB ME - 26A/U SELECTOR: DC. RANGE: 30V. 140A. 1405A (CHENNEL A switches) COUPLING: DC INPUT: ON FUNCTION: A POLARITY: + VERNIER SENSITIVITY: .2. SENS MAG: XI. *142A* SWEEP: MAIN MAGNIFIER: XI NORMAL SINGLE: NORMAL			
2	DELAYED TIME/CM: OFF No change required.....	No change required.....	*a*. Remove ME-26A /U connection from TP8 and connect it to TP6; make note of ME-30A/U indication. b. Adjust 350 D attenuator slowly until ME-26A/U indication changes from -6 volts to +6 volts; make note of indication.	*a*. MF-30A /U should indicate as in 1 *a* above. b. Front panel ALARM lamp should light approximately 2 seconds after ME-26A/U indicates -15 volts; ME-26A/U should indicate 20 dbm less than that recorded in 1 *a* above; DD +205A should indicate excessive distortion.

Step No.	Control; Settings: Test Equipment	Control; Settings: Equipment Under Test	Performance: Test procedure	Performance: standard
			c. Adjust 350 D very slowly, until ALARM indicator lamp is extinguished; make note of ME-30A/U indication.	*c*. ME-30A/U should indicate 10 dbn (±1 dbm) less than indication recorded in 1 *b* above; DD-205A should indicate minimum distortion.
3	No change required.....	No change required	*a*. Connect equipment as shown in A and B, figure 7-3	*a*. ALARM indicator lamp should be extinguished; 140A oscilloscope should indicate a positive 6 volts level ±0.6.
			b. Adjust OUTPUT LEVEL ADJ control slowly until ME-30A/U indicates level recorded in 1 *b* above.	*b*. 140A oscilloscope should indicate a 0-volt level, 2 seconds after level is recorded; the ALARM indicator lamp should be lighted.
			c. Adjust OUTPUT LEVEL ADJ control slowly until ME-30A/U indicates level recorded in I d above.	c. 140A oscilloscope should immediately indicate ±6 volts, -,0.6 ALARM indicator lamp shall be extinguished.
			d. Adjust OUTPUT LEVEL ADJ control slowly until ME-30A/U indication is as in I a above.	*d*. None.
	No change required.....	No change required	a. Remove 140A oscilloscope connection from terminal 13 and connect it to terminal 14 of TB1.	a. 140A oscilloscope should indicate a +6-volt level ±10%.
			b. Adjust 350D attenuator until ME-30A/U indicates level recorded in 2b above.	b. 1 40A oscilloscope should indicate a 0-volt level, 2 seconds after level is reached; ALARM indicator lamp should be lighted.
			c. Adjust 350D attenuator until ME-30A/U indicates level recorded in 2c above.	c. 140A oscilloscope should immediately indicate +6 volts ±10%; ALARM indicator lamp should be extinguished.
				d. None.
	No change required.....	No change required	a. Remove 140A oscilloscope connection from terminal 14 and connect it to terminal 15 of TB1.	a. 140A oscilloscope should indicate a + 6-volt level ±10%.
			b. Remove plug halfway from DAC-7 outputjack.	b. 140A oscilloscope should indicate a 0-volt level, 5 seconds after plug is removed; ALARM indicator lamp should light.
			c. Reinsert plug fully into DAC-7 output jack	c. 140A oscilloscope should indicate a +6-volt level; ALARM indicator lamp should be extinguished.
	No Change required.....	No change required	a. Remove 140A oscilloscope connection from terminal 15 and connect it to terminal 16 of TB1	a. 140A oscilloscope should indicate a +6-vnlt level ±10%.

Step No.	Test Equipment	Control; Settings Equipment Under Test	Test procedure	Performance standard
			b. Remove 350D output wires from terminals 15 and 16 of TB2.	*b*. 140A oscilloscope should indicate a 0-volt level. 5 seconds after wires are removed; ALARM indicator should light.
			c. Reconnect 350D output wires to terminals 15 and 16 of TB2.	*c*. 140A oscilloscope should immediately indicate a +6-volt level, ALARM indicator lamp should be extinguished.

7-9. Summary of Performance Standards

Personnel may find it convenient to arrange the checklist in a manner similar to that shown in *a*, *b,* and *c* below.

a. Data Tests (para 7-6).

Test No.	Description	Performance standard	Test data
1 *a*	Output level	-20 dbm to +3 dbm.	*Mark Space*
1 *c* and *d*	Output Frequency:	0.5 cps of each frequency below:	
		Mark *Space*	
	MX-7372/G	425 595	
	MX-7373/G	510 850	
	MX-7374/G	765 935	
	MX-7375/G	680 1360	
	MX-7376/G	1105 1275	
	MX 7377/G	1190 1530	
	MX-7378/G	1445 1615	
	MX-7379/G	1200 2400	
	MX-7380/G	1785 1955	
	MX-7381/G	1870 2210	
	MX-7382/G	2125 2295	
	MX-7383/G	2040 2720	
	MX-7384/G	2461 2635	
	MX-7385/G	2550 2890	
	MX-7386/G	2805 2975	
1 *e*	No, input signal	No output with maximum distortion.	
2*a*	Input signal with no distortion, looped-back with no attenuation.	Reversal pattern, amplitude of 12 volts ±2.	
2*b*	Input signal with no distortion, looped-back with -35 dbm attenuation.	8% distortion (2% for MX-7379/G).	
2*c*	Input signal with total peak distortion, looped-back with -35 dbm attenuation.	8% distortion (2% for MX-7379/G).	
3*c*	Input signal with total peak distortion. looped-back with + 7 dbm amplification.	3.5% distortion (2% for MX-7379/G).	
3*d*	Input signal with average distortion, looped-back with + 7 dbm amplification.	3.5% distortion (2% for MX-7379/G).	
4*a*	Input signal with 10% spacing bias distortion, looped-back with +7 dbm amplification.	3.5% distortion (2% for MX-7379/G).	
4*b*	Input signal with 10%marking bias distortion, looped-back with + 7 dbm amplification.	3.5% distortion (2% for MX-7379/G).	
4*c*	Input signal with total peak distortion. looped-back with + 7 dbm amplification.	8% distortion (2% for MX-7379/G1.	
4*d*.	Input signal with average distortion, looped-back +7 dbm amplification, TALK REQUEST pushbutton depressed. TALK REQUEST indicator lights.	10% distortion (±29) for 1.5 seconds and the 3.5% (2% for MX-7379/G) ME-26A/U changes from - 15 volts to zero and	
4*e*	Input signal with average distortion, looped-back with +7 dbm amplification. TALK REQUEST RESET pushbutton depressed.	3.5% distortion (2% for MX - 7379/G), ME-26A/U indicates -15 volts and TALK REQUEST indicator extinguishes.	

b. Timing Tests (para 7-7).

Test No.	Description	Performance standard	Test data
1 *a*	Send terminal timing out No.1	Frequency equal to baud rate.	
1 *b*	Send terminal timing out No. 2	Frequency equal to baud rate.	
1 *c*	Receive terminal timing out No.1	Frequency equal to baud rate.	
1 *d*	Receive terminal timing out No. 2	Frequency equal to baud rate.	
1 *e*	Data and send timing comparison	Data and timing are same frequency but not necessarily synchronized.	
1 *f*	Data and receive timing comparison .	Data and timing synchronized.	
1 *g*	lower removed and reapplied	Data and timing synchronized.	
2 *b*	Power removed and reapplied internal clock).	Data and timing synchronized.	

c. Alarm Tests (para 7-8).

Test No.	Description	Performance standard	Test data
1*a*.....	Transmit output level	20 dbm to + 3 dbm.	
1*b*.....	Transmit signal alarm	ALARM indicator lights 2 seconds after ME-26A/U indicates volts.- 15 volts.	
1*c*.....	Signal decrease.....	10 dbm less than 1*a* above.	
1*d*.....	Signal increase.....	5 dbm ±1 less than 1*a* above with ALARM indicator extinguished.	
2*a*.....	Receive signal alarm.....	-20 dbm to + 3 dbm.	
2*b*.....	Signal decrease.....	ALARM indicator lights 2 seconds after ME-26A/U indicates -15 volts and ME-30A/U indicates 20 dbm less than 2*a* above.	
2*c*.....	Signal increase.....	10 dbm ±1 less than 2*a* above with minimum distortion.	
3*a*.....	LOSS OF XMTR CARRIER ALARM terminal output level.	ALARM indicator extinguished and 140A indicates + 6 volts ±0.6.	
3*b*.....	Signal decrease.....	ALARM indicator lights and 140A indicates zero 2 seconds after ME-30A/U indicates as in 1*c* above.	
3*c*.....	Signal increase.....	ALARM indicator extinguishes and 140A indicates +6 volts ±`0.6.	
4*a*.....	LOSS OF REC CARRIER ALARM terminal output level.	ALARM indicator extinguished and 140A indicates +6 volts ±0.6.	
4*b*.....	Signal decrease.....	ALARM indicator lights and 140A indicates zero 2 seconds after ME-30A/U indicates as in 1*c* above.	
4*c*.....	Signal increase.....	ALARM indicator extinguishes and 140A indicates +6 volts ±0.6.	
5*a*.....	NO TRANSITION ALARM SEND terminal output level.	ALARM indicator extinguished and 140A indicates +6 volts ±0.6.	
5*b*.....	Signal removed.....	ALARM indicator lights and 140A indicates zero 5 seconds after signal is removed.	
5*c*.....	Signal applied.....	ALARM indicator extinguishes and 140A indicates +6 volts ±0.6.	
6*a*.....	NO TRANSITION ALARM REC terminal output level.	ALARM indicator extinguished and 140A indicates + 6 volts ±0.6.	
6*b*.....	Signal removed.....	ALARM indicator lights and 140A indicates zero 5 seconds after signal is removed.	
6*c*.....	Signal applied.....	ALARM indicator extinguishes and 140A indicates +6 volts ±0.6.	

CHAPTER 8

ADJUSTMENTS AND FINAL TESTING

8-1. General

a. All necessary adjustments for the MD674(P)/G should be performed with the equipment in a normal operating environment. However, the individual adjustments may be made on *a bench operated* equipment, and then, if necessary, *touched-up* after the equipment is placed into operation. The necessary adjustments include the demodulator bias adjustment and the transmit and receive alarm circuit adjustments, and order-wire circuit and oscillator adjustments.

b. The final testing procedures to check to see that required equipment meets the minimum standards of new equipment are the same as described for general support testing in chapter 7.

8-2. Crystal Oscillator and Oven Assembly Module

a. General. To adjust the two oscillators in the crystal oscillator and oven assembly, the cover of the assembly (fig. 2-6) must be removed to gain access to the variable inductors. Adjustment of the individual crystal oscillator is performed by adjusting the inductor until the oscillator starts. The output frequency is then checked to see if it is within 35 cycles of the required frequency. The chart in c below lists the required mark and space frequencies for each MX-73(*)/G.

CAUTION

Bending of pin 3 can short out the oscillator signal, causing equipment damage or incorrect reading. Ensure that this pin is not bent by connected test probes.

b. Procedure (fig. 6-21).

(1) With the cover removed from the crystal oscillator and oven assembly, connect the 140A oscilloscope between pin 3 (signal) and pin 5 (ground) of PC 80034210.

(2) Operate the AC POWER, switch to ON, and adjust inductor L1 (mark oscillator) until the oscillator starts (indicated by output waveform on the 140A oscilloscope).

(3) Operate the AC POWER switch to off and then to ON.

(4) If there is any delay in starting of the oscillator, adjust inductor L1 and repeat the procedure in (3) above until the oscillator produces an output with minimum delay after the AC POWER switch is operated from off to ON.

(5) Connect the 140A oscilloscope between pins 4 (signal) and 5 (ground) of PC 80034210, and repeat the procedures in (2), (3), and (4) above to adjust the space oscillator.

(6) After the adjustments are made as described above, connect the 5233L electronic counter to pins 3 and 5 (mark oscillator) and then to pins 4 and 5 (space oscillator) and check to see that the output frequencies are within 35 cps of the frequencies indicated in the chart in c below.

(7) Replace oven cover.

(8) Check oven temperature and adjust, if required, in accordance with *d* below.

c. Oscillator Frequency Chart.

MX-73(*)/G	Mark oscillator frequency (ke)	Space oscillator frequency (kc)
MX-7372/G ----------	217.600	304.640
MX-7373/G ----------	261.120	435.200
MX-7374/G ----------	195.840	239.360
MX-7375/G ----------	174.080	348.160
MX-7376/G ----------	282.880	326.400
MX-7377/G ----------	152.320	195.840
MX-7378/G ----------	184.960	206.720
MX-7379/G ----------	153.600	307.200
MX-7380/G ----------	228.480	250.240
MX-7381/G ----------	239.360	282.880
MX-7382/G ----------	272.000	293.760
MX-7383/G ----------	261.120	348.160
MX-7384/G ----------	157.760	168.640
MX-7385/G ----------	163.200	184.960
MX-7386/G ----------	179.520	190.400

d. Oven Temperature Adjustment.

(1) Insert thermocouple probe of temperature tester (Simpson Model 388-3L), NSN 6685-00-975-4544, into oven through screw hole in top cover.

(2) Observe oven temperature until a stable reading is obtained. If not 750 C proceed to (3) below.

(3) Adjust OVEN TEMP ADJUST control R1 over a period of 10 minutes to obtain a 75°C reading on the temperature tester. Lock setting of R1 and apply a drop of glyptal varnish to shaft.

(4) Remove probe from oven and replace screw in top cover.

e. Waveform Adjustment. Connect oscilloscope to J1 of modem subassembly A 18A2 through A29A2. These subassemblies are inserted into the same slot and use of each is determined by the operating frequency. If the subassembly is not inserted into the slot because of low operating frequency, connect the oscilloscope to J1 of subassembly A7. The desired waveform is shown in A of figure 8-2. An undesirable waveform, that shows a distorted and unstable lagging edge is shown in B. Attempt to correct the distorted waveform by adjusting L1. If the distortion cannot be adjusted replace the oscillator and oven assembly (para 4-6).

8-2.1. Adjustment of Variable Control Oscillator (VCO)

a. Strap assembly Al for external clock operation by connecting TP4 and TP5 together and terminals 1 and 2 together.

b. Connect the HP-5233L Counter between SEND TERMINAL TIMING OUT #2 terminal 1 of TB2 and ground terminal 11 of TB2.

c. Set the BAUD RATE switch to 1200.

d. With no external timing signal applied and power applied to the unit, adjust inductor L1 on assembly A1 (fig. 6-2) until the HP-5233L counter indicates between 1,215 Hz and 1,200 Hz.

e. Connect the external timing signal (150-, 300-, 600-, or 1,200-Hz) between RECEIVER EXTERNAL TIMING INPUT terminal 7 of TB1 and RETURN terminal 8 of TB1.

NOTE

If the return line is not grounded at the signal source, connect a jumper between RETURN terminal 8 and terminal 11 of TB2.

f. Set the BAUD RATE switch to the appropriate position (as determined by the input signal frequency) and observe that the HP-5233L counter indicates the frequency of the external timing frequency.

8-3. Demodulator Bias Adjustment

a. General. The demodulator bias adjustment is performed with an undistorted data input signal applied to the transmit input circuit, and the equipment connected in a loop-back configuration (para 2-7). Best results are obtained with the MD-674(P)/G operating in the unretimed data mode.

b. Adjustment Procedures.

(1) Connects a data-source (such as the DAC-6A Pattern Generator) to the front panel ORDER WIRE SEND jack.

(2) Connect the 140A oscilloscope between test jack J2 on PC assembly A8 (fig. 6-27) and ground.

(3) Strap, together, terminals 2 and 4 on PC assembly A11 to obtain the unretimed mode of operation.

(4) With power and data signals applied, set the INPUT SELECT switch (fig. 2-3) to DATA and adjust the 140A oscilloscope for a crossover pattern.

(5) Adjust the BIAS ADJUST control until a zero-bias crossover pattern is observed on the 140A oscilloscope.

8-4. Alarm Adjustments

a. General. All alarm adjustments are made with transmit data applied and the MD-674(P)/G connected in a loop-back configuration (para 2-7). Both receive and transmit carrier alarm circuits require two adjustments: The threshold adjustment and a delay time to activate adjustment. The no-transition alarms require only one adjustment.

b. Transmit Carrier Alarm Adjustments.

(1) Connect the ME-26A/U between test point TP8 (on the control shelf, fig. 2-3) and ground.

(2) Check the transmit output level by connecting the ME-30A/U to BALANCED XMTR CARRIER OUTPUT terminals 12 and 13 on terminal board TB2 at the rear of the equipment (fig. 1-8).

(3) If necessary, adjust the front panel OUTPUT LEVEL ADJ control for an optimum -7dBm output level.

(4) Adjust the OUTPUT LEVEL ADJ control for a - 17dBm output level (alarm condition); the ME-26A/U should indicate -15 volts.

(5) If the ME-26A/U does not indicate -15 volts, adjust the XMIT CARRIER ALARM THRESHOLD control (fig. 2-3) until the ME26A/U indicates -15 volts.

(6) Adjust the output level for -7 dbm, as indicated by the ME-30A/U, and connect the ME-26A/U between test point TP9 (fig. 2-3) and ground; the ME-26A/U should indicate approximately -6 volts.

(7) Adjust the OUTPUT LEVEL ADJ control for -17dBm output level, and check for a 2-second delay before the ME-26A/U indicates +6 volts.

(8) If the +6 volts indication does not occur exactly 2 seconds after the alarm condition occurs, adjust the OUTPUT LEVEL ADJ control for a -7dBm indication on the ME-26A/U; then rotate the XMIT CARRIER ALARM TIME control slightly (clockwise if the time delay is too long, counterclockwise if the time delay is too short) and repeat the procedure in (4) above.

(9) Continue to perform the procedures in (8) and (4) above until the ME-26A/U provides a +6 volts indication exactly 2 seconds after the output level is decreased to -17 dbm.

(10) Adjust the OUTPUT LEVEL ADJ control for a -12-dbm indication on the ME-30A/U; the ME-26A/U should indicate -6 volts, immediately.

Note. The alarm condition (+6 volts indication on ME-26A/U) must occur 2 seconds after the output level has decreased 10 dbm from normal. If an output level other than -7 dbm is to be used, obtain the alarm condition by decreasing that output level by 10 dbm, and remove the alarm condition by then raising the output level by 5 dbm. *For example*, if the desired output level is 0 dbm, the alarm condition should occur at -10 dbm, and reset at -5 dbm. Do not set the output level for less than -10 dbm or an alarm condition will never be reached.

c. Receiver Carrier Alarm Adjustments.

(1) Connect the ME-26A/U between test point TP5 on the control shelf (fig. 2-3) and ground.

(2) Connect the BALANCED TRANSMIT CARRIER OUTPUT terminals (13 and 14 on TB2 at the rear of the equipment, fig. 1-8), through the 350D attenuator, to the BALANCED RECEIVE CARRIER INPUT terminals (15 and 16 on TB2).

(3) Connect the ME-30A/U to terminals 15 and 16 on TB2, and adjust the 350D attenuator for a -10-dbm indication on the ME-30A/U.

Note. This is a normal input level value and should be used as much as possible. Never can the receive input level be less than -15 dbm.

(4) Adjust the 350D attenuator for a -30-dbm indication on the ME-30A/U (alarm condition); the ME-26A/U should indicate +6 volts after the -30-dbm level is reached.

(5) If the ME-26A/U does not indicate +6 volts, adjust the REC CARRIER ALARM THRESHOLD control (fig. 2-3) until the ME-26A/U indicates +6 volts.,

(6) Set the input level to -10-dbm level, as indicated by the ME-30A/U , and connect the ME-26A/U between test point TP6 (fig. 2-3) and ground: the ME-26A/U should indicate approximately -6 volts.

(7) Adjust the 350D attenuator for a -30-dbm output level, and check for a 2-second delay before the ME-26A/U indicates +6 volts.

(8) If the +6-volt indication does not occur exactly 2 seconds after the alarm condition occurs, adjust the 350D attenuator for a -10-dbm indication on the ME30A/U; then rotate the REC CARRIER ALARM TIME control slightly (clockwise if the delay time is too long; counterclockwise if the time is too short) and repeat the procedure in (4) above.

(9) Continue to perform the procedures in (8) and (4) above until the ME-26A/U provides a +6-volt indication exactly 2 seconds after the input level is decreased to -30 dbm.

(10) Adjust the 350D attenuator for a -20 dbm indication on the ME-30A/U; the ME-26A/U should indicate -6 volts immediately.

Note. The alarm condition (+6 volts indication on the ME-26A/U must occur 2 seconds after the input level has decreased 20 dbm from normal. If an input level other than -10 dbm is to be used, obtain the alarm condition by decreasing the input level by 20 dbm, and remove the alarm condition by then increasing the input level by 10 dbm. *For example*, if the desired input level is -6 dbm, the alarm condition should occur at -26 dbm and reset at -16 dbm.

d. No-Transition Alarm Send.

(1) Connect the ME-26A/U between test point TP2 on the control shelf (fig. 2-3) and ground; the ME-26A/U should indicate -3.84 volts approximately.

(2) Set the INPUT SELECT switch to OFF (alarm condition), and check for a 5-second delay before the ME-26A/U indicates +6 volts.

(3) If the +6-volt indication does not occur exactly 5 seconds after the alarm condition occurs, set the INPUT SELECT switch to DATA; then adjust the TRANSITION ALARM TIME TRANSMIT control, on the control bracket, slightly (clockwise if the time delay is too long; counterclockwise if the time delay is too short) and repeat the procedure in (2) above.

(4) Continue to perform the procedures in (3) and (2) above until the ME-26A/U

provides at +6-volt indication exactly 5 seconds after the INPUT SELECT switch is operated from DATA to OFF.

e. No-Transition Alarm Receive.

(1) Connect the ME-26A/U between test point TP1 on the control shelf (fig. 2-3) and ground; the ME-26A/U should indicate -3.84 volts approximately.

(2) Repeat the procedures in *d*(2), (3), and (4) above, adjusting the TRANSITION ALARM TIME RECEIVE control in place of the TRANSITION ALARM TIME TRANSMIT control.

8-5. Order-Wire Circuit Adjustments

a. Connect the ME-26A/U between test point TP3 on the control shelf (fig. 2-3) and ground; the ME-26A/U should indicate + 15 volts.

b. Depress the front panel TALK REQUEST pushbutton. and check for a 1-second delay before the ME-26A/U indicates 0 volt.

c. If the 0-volt indication does not occur exactly 1 second after the TALK REQUEST pushbutton is depressed, adjust the TALK REQUEST DELAY control (fig. 2-3) slightly (clockwise if the time delay is too long; counterclockwise if the time delay is too short); then depress the TALK REQUEST RESET pushbutton, and repeat the procedure in *b* above.

d. Continue to perform the procedures in *c* and *d* above until the ME-26A/U provides a 0-volt indication exactly 1 second after the TALK REQUEST pushbutton is depressed.

e. Connect the ME-26A/U between test point TP4, on the control shelf and ground; the ME-26A/U should indicate 0 volt.

f. Depress the front panel TALK REQUEST pushbutton, and check for a 1.75-second delay before the ME-26A/U indicates +6 volts.

g. If the +6-volt indication does not occur exactly 1.75 seconds after the TALK REQUEST pushbutton is depressed, adjust the TALK REQUEST WINDOW control (fig. 2-3) slightly (clockwise if the time delay is too long; counterclockwise if the time delay is too short); then depress the TALK REQUEST RESET pushbutton, and repeat the procedure in *f* above.

h. Continue to perform the procedures in *g* and *f* above until the ME-26A/U provides a + 6-volts indication exactly 1.75 seconds after the TALK REQUEST pushbutton is depressed.

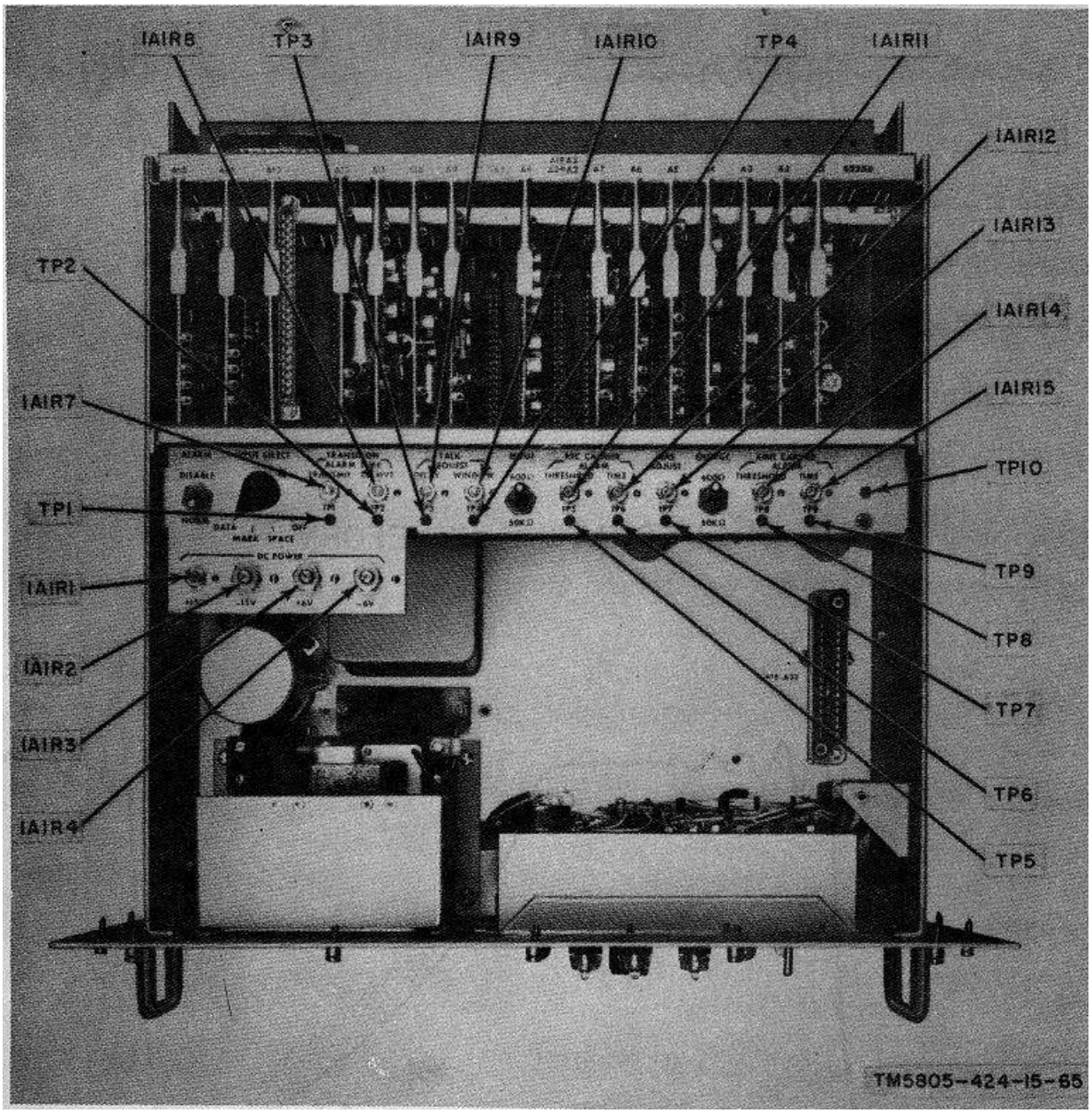


Figure 8-1. Modem, Low Speed Wire Line MD-674(*)/G, removed from case, top view, Less Modem Subassembly MX-73(*)/G and Clock Module Group OA-8072/G, adjustment at locations.

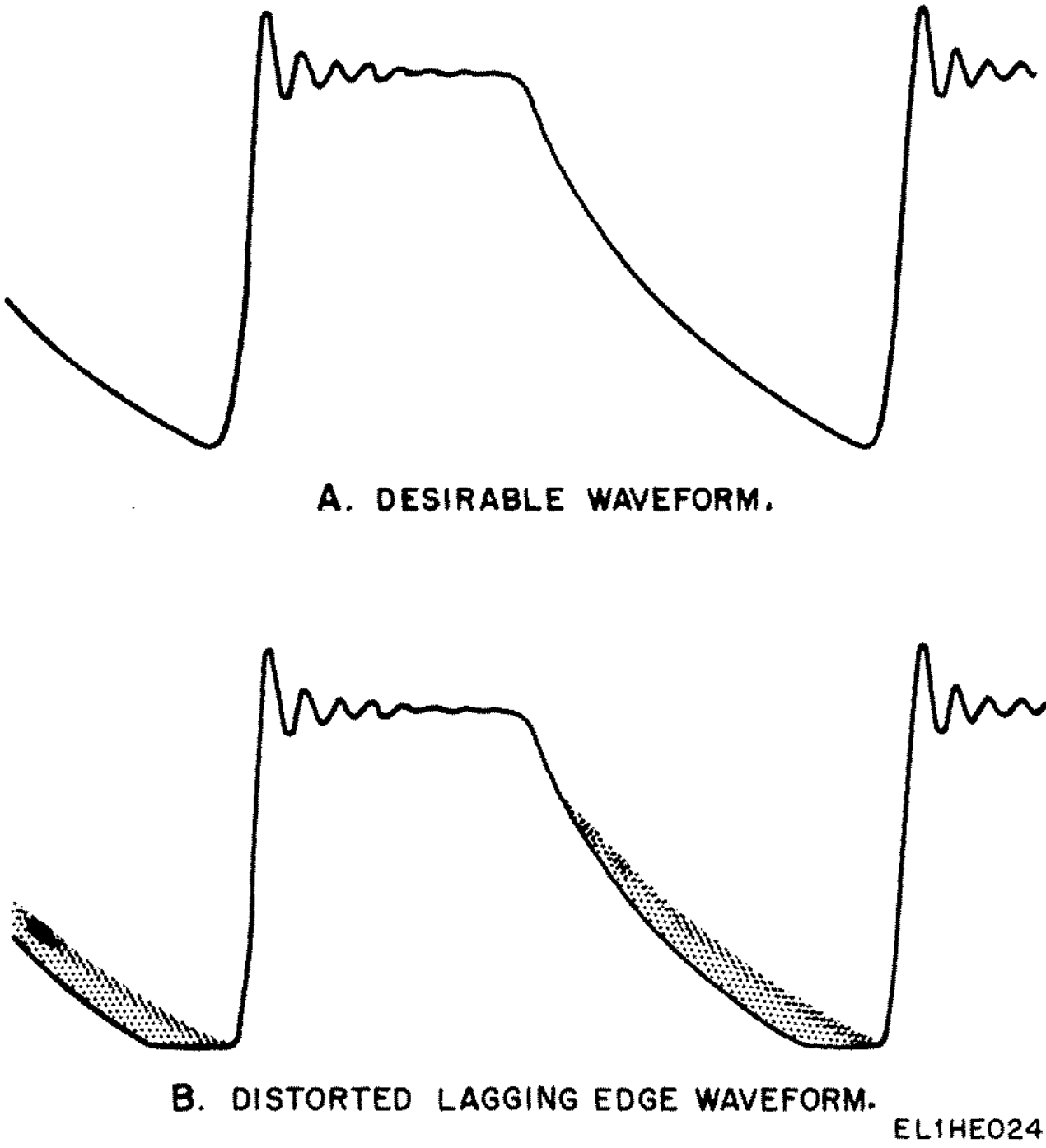


Figure 8-2. Frequency determining module (FDM) waveform check.

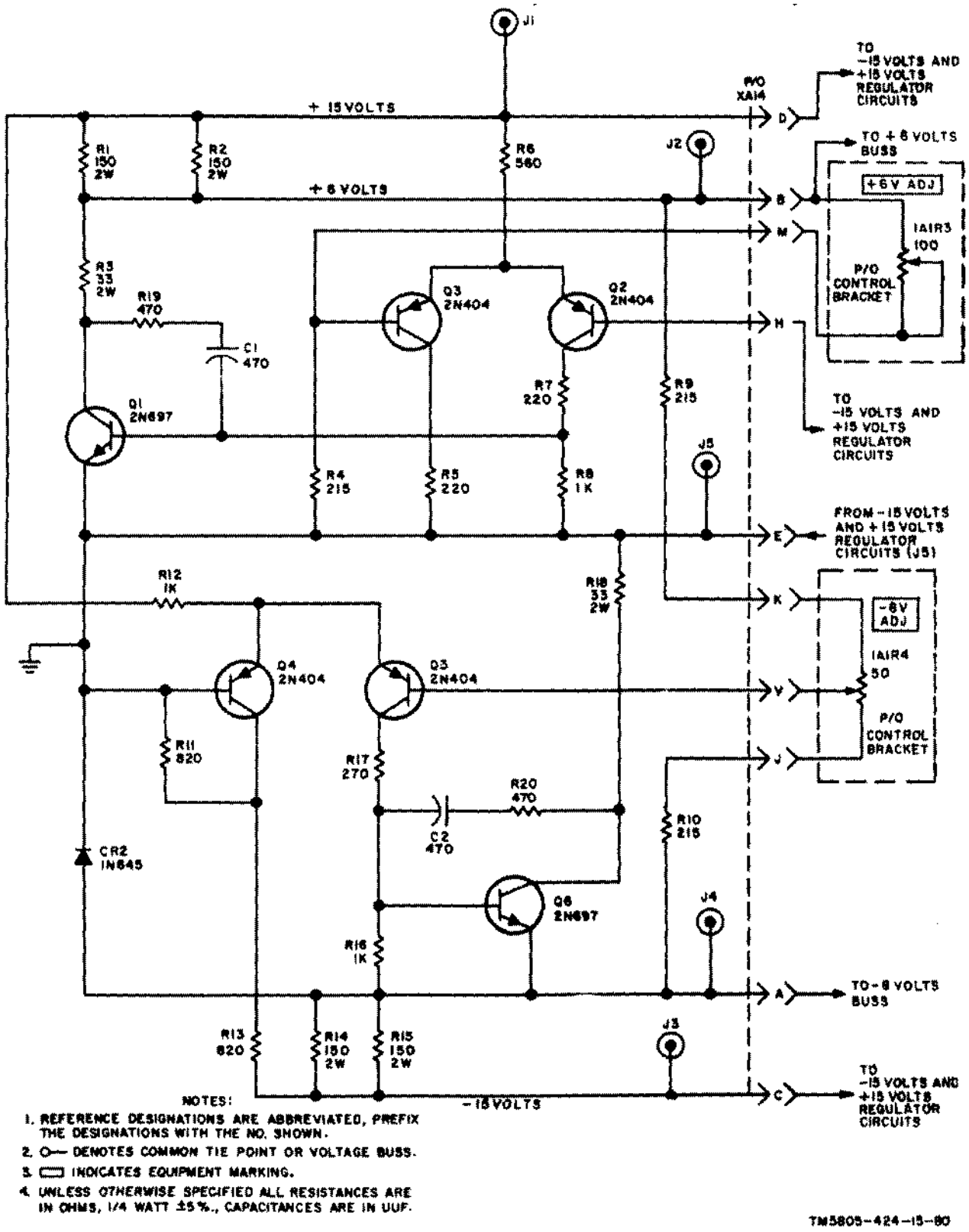


Figure 8-18. ±6 volt power supply regulator circuits assembly A14 (PC 80034170), schematic diagram.

CHAPTER 8.1

PAGES 8.1-1 AND 8.1-2 ARE UNAVAILABLE FOR DIGITIZATION

8.1-1/8.1-2

8.1-5. Input Capacitance Tests

The purpose of the input capacitance test is to determine if optimum input voltage is obtained. Perform the following procedures:

a. Connect the equipment as shown in figure 8.1-2.

b. Operate the AC POWER ON-OFF switch to ON.

c. Adjust the capacitance decade box until optimum wave is displayed on the scope. The capacitance value should not exceed 1,500 pica-farads on the decade capacitance box.

8.1-6. Output Impedance Tests

The purpose of the output impedance tests is to determine that the output impedance does not exceed 100 ohms maximum. Perform the following procedures:

a. Connect the equipment as shown in figure 8.1-3.

b. Operate the AC POWER ON-OFF switch to ON.

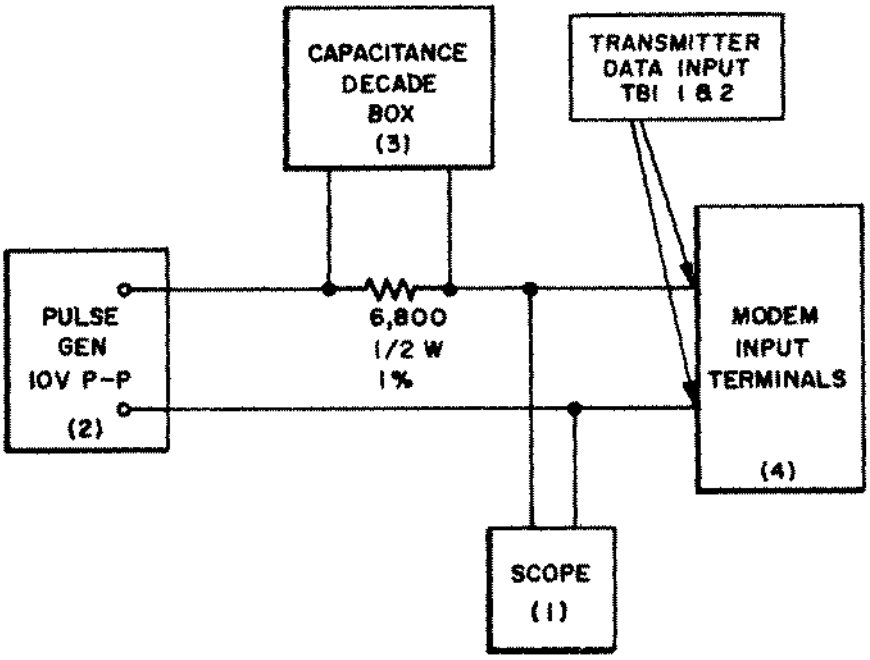
c. Measure the output voltage without a load (V1).

d. Measure the output voltage with the 1,360 ohm load (V2).

e. Calculate the output impedance as follows:

$$Z\ OUT = \frac{V1 - V2}{V2}$$

f. The output impedance should not exceed 100 ohms maximum.



LEGEND:
1. OSCILLOSCOPE AN/USM-1406
2. PULSE GENERATOR AN/UPM-15A
3. CAPACITOR, DECADE AN/URM-2
4. MODEM, LOW SPEED WIRE LINE MD-674 (P)/G

TM5805-424-15-C1-2

Figure 8.1-2. Connections for input capacitance tests.

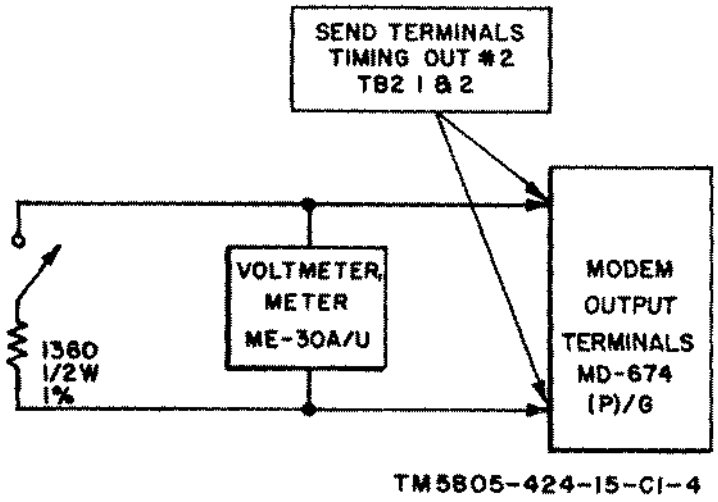


Figure 8.1-3. Connections for output impedance tests.

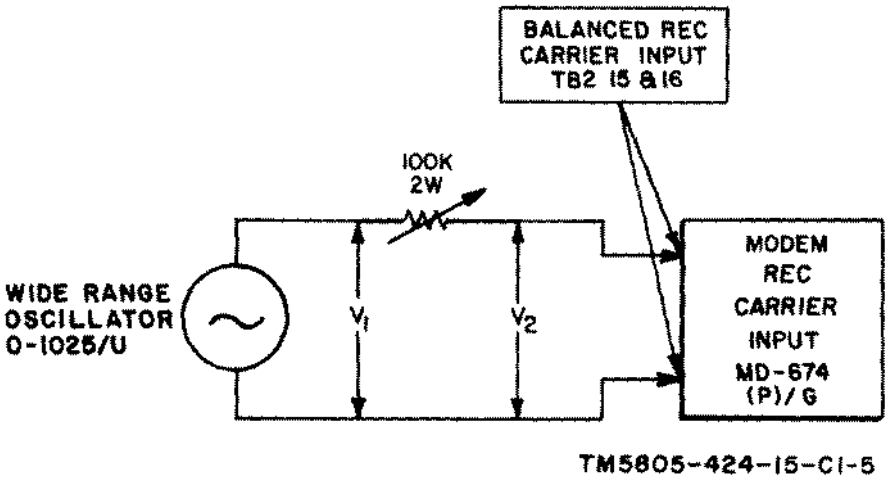


Figure 8.1-4. Connections for input impedance tests.

8.1-7. Input Impedance Tests

The purpose of the input impedance tests is to check to see that input impedances are 600 ohms and 50,000 ohms by performing the following procedures:

a. 50,000-Ohm Terminator.

(1) Connect the equipment as shown in figure 8.1-4.

(2) Operate the POWER switch to ON.

(3) Operate the 600-ohm termination switch to out.

(4) Set the value of R to 50,000 ohms.

(5) Set the SG-15/PCM to an output level of 1 volt rms at 1,000 hz.

(6) Measure the voltage (V2); it must be greater than 0.5 volt rms.

b. 600-Ohm Termination.

(1) Operate the POWER switch to ON.

(2) Operate the 600-ohm termination switch to out and repeat *a*(5) above.

(3) Set the value of R to make the voltage (V2) exactly one-half that of V1.

(4) Measure the value of R; it must be 600 ohms ±10 percent.

(5) Repeat the procedures given in a above and (1) through (4) above using 300 hz and 3,400 hz.

8.1-8. Input Resistance Test

The purpose of the input resistance test is to determine whether the MD-674(P)/G has the proper input resistance by performing the following procedures:

a. Connect the equipment as shown in figure 8.1-5; set the ME-30A/U, connected across the 1K resistor to read 1 volt, full scale.

b. Operate the ON-OFF switch to ON.

c. Adjust the voltage source until the ME-30A/U across the MD-674(P)/G input terminals reads 6 volts.

d. The ME-30A/U across the 1K resistor should read between 0.80 and 0.98 volt.

e. Reverse the polarity on the transmitter data input terminals and repeat the procedure given in *d* above.

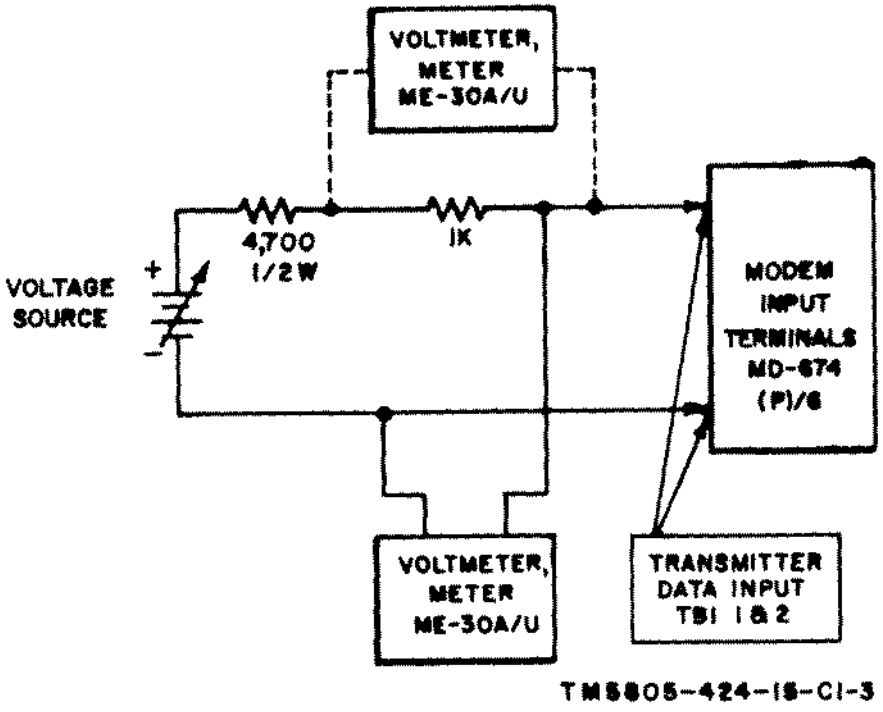


Figure 8.1-5. Connections for input resistance tests.

APPENDIX A

REFERENCES

AR 380-40	Policy for Safeguarding and Controlling COMSEC Information (U).
AR 735-11-2	Reporting of Item and Packaging Discrepancies.
DA Pam 310-1	Consolidated Index of Army Publications and Blank Forms.
DA Pam 738-750	The Army Maintenance Management System (TAMMS).
FM 11-62	Communications-Electronics Fundamentals: Solid State Devices and Solid State Power Supplies.
SB 38-100	Preservation, Packaging, Packing and Marking Materials, Supplies and Equipment Used by the Army.
TB SIG 222	Solder and Soldering.
TB 43-0118	Field Instructions for Painting and Preserving Electronics Command Equipment Including Camouflage Pattern Painting of Electrical Equipment Shelters.
TM 11-5805-424-20P	Organizational Maintenance Repair Parts and Special Tools Lists for Modem, Low Speed Wire Line, MD-674(P)/G (NSN 5805-00-963-4888).
TM 11-5805-424-34P	Direct Support and General Support Maintenance Repair Parts and Special Tools Lists (Including Depot Maintenance Repair Parts and Special Tools) for Modem, Low Speed Wire Line, MD-674(P)/G (NSN 5805-00-963-4888).
TM 11-6625-200-15	Operator's, Organizational, Direct Support, General Support, and Depot Maintenance Manual: Multimeters ME-26A/U (NSN 6625-00-360-2493), ME-26B/U, ME-26C/U (NSN 6625-00-646-9409), and ME-26D/U (NSN 6625-00-913-9781).
TM 11-6625-320-12	Operator's and Organizational Maintenance Manual: Voltmeter, Meter, ME-30A/U and Voltmeters, Electronic, ME-30B/U and ME-30C/U and ME-30E/U.
TM 740-90-1	Administrative Storage of Equipment.
TM 750-244-2	Procedures for Destruction of Electronics Materiel to Prevent Enemy Use (Electronics Command).

APPENDIX B

MAINTENANCE ALLOCATION

Section I. INTRODUCTION

B-1. General

This appendix provides a summary of the maintenance operations for MD-674(P)/G. It authorizes categories of maintenance for specific maintenance functions on repairable items and components and the tools and equipment required to perform each function. This appendix may be used as an aid in planning maintenance operations.

B-2. Maintenance Function

Maintenance functions will be limited to and defined as follows:

a. Inspect. To determine the serviceability of an item by comparing its physical, mechanical, and/or electrical characteristics with established standards through examination.

b. Test. To verify serviceability and to detect incipient failure by measuring the mechanical or electrical characteristics of an item and comparing those characteristics with prescribed standards.

c. Service. Operations required periodically to keep an item in proper operating condition; i.e., to clean (decontaminate), to preserve, to drain, to paint, or to replenish fuel, lubricants, hydraulic fluids, or compressed air supplies.

d. Adjust. To maintain, within prescribed limits, by bringing into proper or exact position, or by setting the operating characteristics to the specified parameters.

e. Align. To adjust specified variable elements of an item to bring about optimum or desired performance.

f. Calibrate. To determine and cause corrections to be made or to be adjusted on instruments or test measuring and diagnostic equipments used in precision measurement. Consists of comparisons of two instruments, one of which is a certified standard of known accuracy, to detect and adjust any discrepancy in the accuracy of the instrument being compared.

g. Install. The act of emplacing, seating, or fixing into position an item, part, module (component or assembly) in a manner to allow the proper functioning of the equipment or system.

h. Replace. The act of substituting a serviceable like type part, subassembly, or module (component or assembly) for an unserviceable counterpart.

i. Repair. The application of maintenance services (inspect, test, service, adjust, align, calibrate, replace) or other maintenance actions (welding, grinding, riveting, straightening, facing, remachining, or resurfacing) to restore serviceability to an item by correcting specific damage, fault, malfunction, or failure in a part, subassembly, module (component or assembly), end item, or system.

j. Overhaul. That maintenance effort (service/action) necessary to restore an item to a completely serviceable/operational condition as prescribed by maintenance standards (i.e., DMWR) in appropriate technical publications. Overhaul is normally the highest degree of maintenance performed by the Army. Overhaul does not normally return an item to like new condition.

k. Rebuild. Consists of those services/actions necessary for the restoration of unserviceable equipment to a like new condition in accordance with original manufacturing standards. Rebuild is the highest degree of materiel maintenance applied to Army equipment. The rebuild operation includes the act of returning to zero those age measurements (hours, miles, etc.) considered in classifying Army equipments/components.

B-3. Column Entries

a. Column 1, Group Number. Column 1 lists group numbers, the purpose of which is to identify

components, assemblies, subassemblies, and modules with the next higher assembly.

b. Column 2, Component/Assembly. Column 2 contains the noun names of components, assemblies, and modules for which maintenance is authorized.

c. Column 3, Maintenance Functions. Column 3 lists the functions to be performed on the item listed in column 2. When items are listed without maintenance functions, it is solely for purpose of having the group numbers in the MAC and RPSTL coincide.

d. Column 4, Maintenance Category. Column 4 specifies, by the listing of a "work time" figure in the appropriate subcolumn(s), the lowest level of maintenance authorized to perform the function listed in column 3. This figure represents the active time required to perform that maintenance function at the indicated category of maintenance. If the number or complexity of the tasks within the listed maintenance function vary at different maintenance categories, appropriate "work time" figures will be shown for each category. The number of task-hours specified by the "work time" figure represents the average time required to restore an item (assembly, subassembly, component, module, end item or system) to a serviceable condition under typical field operating conditions. This time includes preparation time, troubleshooting time, and quality assurance/quality control time in addition to the time required to perform the specific tasks identified for the maintenance functions authorized in the maintenance allocation chart. Subcolumns of column 4 are as follows:

C-Operator/Crew
O-Organizational
F-Direct Support
H-General Support
D-Depot

e. Column 5, Tools and Equipment. Column 5 specifies by code, those common tool sets (not individual tools) and special tools, test, and support equipment required to perform the designated function.

f. Column 6, Remarks. Column 6 contains an alphabetic code which leads to the remark in section IV, Remarks, which is pertinent to the item opposite the particular code.

B-4. Tool and Test Equipment Requirements (Sec III)

a. Tool or Test Equipment Reference Code. The numbers in this column coincide with the numbers used in the tools and equipment column of the MAC. The numbers indicate the applicable tool or test equipment for the maintenance functions.

b. Maintenance Category. The codes in this column indicate the maintenance category allocated the tool or test equipment.

c. Nomenclature. This column lists the noun name and nomenclature of the tools and test equipment required to perform the maintenance functions.

d. National/NATO Stock Number. This column lists the National/NATO stock number of the specific tool or test equipment.

e. Tool Number. This column lists the manufacturer's part number of the tool followed by the Federal Supply Code for manufacturers (5 digit) in parentheses.

B-5. Remarks (Sec IV)

a. Reference Code. This code refers to the appropriate item in section II, column 6.

b. Remarks. This column provides the required explanatory information necessary to clarify items appearing in section II.

SECTION II MAINTENANCE ALLOCATION CHART
FOR
MODEM, LOW SPEED WIRE LINE MD-674(P)/G

(1) GROUP NUMBER	(2) COMPONENT/ ASSEMBLY	(3) MAINT. FUNCTION	(4) MAINTENANCE CATEGORY C	O	F	H	D	(5) TOOLS AND EQUIP	(6) REMARKS
00	Modem., Low Speed Wire Line HD-674(P)/G	Inspect		0.5					
		Test		1.0				1 thru 3	A
		Test			2.0			1 thru 10	
		Service		0.5				3	
		Adjust				1.0		1 thru 14	
		Replace		0.5				1 thru 3	
		Repair		1.0				1 thru 3	A
		Repair			2.0			1 thru 10	
		Overhaul					20.0	1 thru 22	
01	Chassis, Electrical Equipment 1A1	Inspect		0.3					
		Test		0.5				1 thru 3	
		Repair			1.0			1,2,5	
0101	Modem Subassembly, 1A1A1	Inspect		0.2					
		Test		0.5				1 thru 3	
		Replace		0.5				1 thru 3	
		Repair					2.0	1 thru 22	
0102	Modem Subassembly, 1A1A2	Inspect		0.2					
		Test		0 5				1 thru 3	
		Replace		0.5				1 thru 3	
		Repair					2.0	1 thru 22	
0103	Modem Subassembly, 1A1A3	Inspect		0.2					
		Test		0.5				1 thru 3	
		Replace		0.5				1 thru 3	
		Repair					2.0	1 thru 22	
0104	Modem Subassembly, 1A1A4	Inspect		0.2					
		Test		0.5				1 thru 3	
		Replace		0.5				1 thru 3	
		Repair					2.0	1 thru 22	
0105	Modem Subassembly, 1A1A5	Inspect		0.2					
		Test		0.5				1 thru 3	
		Replace		0.5				1 thru 3	
		Repair					2.0	1 thru 22	
0106	Modem Subassembly, 1A1A6	Inspect		0.2					
		Test		0.5				1 thru 3	
		Replace		0.5				1 thru 3	
		Repair					2.0	1 thru 22	
0107	Modem Subassembly, 1A1A7	Inspect		0.2					
		Test		0.5				1 thru 3	
		Replace		0.5				1 thru 3	
		Repair					2.0	1 thru 22	
0108	Modem Subassembly, 1A1A8	Inspect		0.2					
		Test		0.5				1 thru 3	
		Replace		0.5				1 thru 3	
		Repair					2.0	1 thru 22	
0109	Modem Subassembly, 1A1A9	Inspect		0.2					
		Test		0.5				1 thru 3	
		Replace		0.5				1 thru 3	
		Repair					2.0	1 thru 22	
0110	Modem Subassembly, 1A1A10	Inspect		0.2					
		Test		0.5				1 thru 3	
		Replace		0.5				1 thru 3	
		Repair					2.0	1 thru 22	
0111	Modem Subassembly, 1A1A11	Inspect		0.2					
		Test		0.5				1 thru 3	
		Replace		0.5				1 thru 3	
		Repair					2.0	1 thru 22	
0112	Modem Subassembly, 1A1A12	Inspect		0.2					
		Test		0.5				1 thru 3	
		Replace		0.5				1 thru 3	
		Repair					2.0	1 thru 22	

SECTION II MAINTENANCE ALLOCATION CHART
FOR
MODEM, LOW SPEED WIRE LINE MD-674(P)/G

(1)	(2)	(3)	(4) MAINTENANCE CATEGORY					(5)	(6)
GROUP NUMBER	COMPONENT/ ASSEMBLY	MAINT. FUNCTION	C	O	F	H	D	TOOLS AND EQUIP	REMARKS
0113	Modem Subassembly, 1A1A13	Inspect		0.2					
		Test		0.5				1 thru 3	
		Replace		0.5				1 thru 3	
		Repair					2.0	1 thru 22	
0114	Modem Subassembly, 1A1A14	Inspect		0.2					
		Test		0.5				1 thru 3	
		Replace		0.5				1 thru 3	
		Repair					2.0	1 thru 22	
0115	Modem Subassembly, 1A1A15	Inspect		0.2					
		Test		0.5				1 thru 3	
		Replace		0.5				1 thru 3	
		Repair					2.0	1 thru 22	
0116	Modem Subassembly, 1A1A16	Inspect		0.2					
		Test		0.5				1 thru 3	
		Replace		0.5				1 thru 3	
		Repair					2.0	1 thru 22	
0117	Power Supply, 1A1A17	Inspect		0.2					
		Test		0.5				1 thru 3	
		Replace		0.5				1 thru 3	
		Repair			2.0			1 thru 10	
0118	Clock Module Group OA-8072/G, 1A1A33								
011801	Clock Module Subassembly, 1A1A33A2	Inspect		0.2					
		Test		0.5				1 thru 3	
		Replace		0.5				1 thru 3	
		Repair					2.0	1 thru 22	
011802	Oscillator, RF, 1A1A33A1	Inspect		0.2					
		Test		0.5				1 thru 3	
		Replace		0.5				1 thru 3	
0119	Modem Subassembly MX-7372/C, 1A1A18	Inspect		0.3					
		Test		0.5				1 thru 3	A
		Test				1.0		1 thru 14	
		Adjust				1.0		1 thru 14	
		Replace		0.3				1 thru 3	
		Repair				2.0		1 thru 14	
011901	Electrical Component Assembly, 1A1A18TB1	Test				0.5		1 thru 14	B
		Test					1.0	1 thru 22	
		Replace				1.0		1 thru 14	
		Repair					2.0	1 thru 22	
011902	Modem Subassembly, 1A1A18A2	Test		0.5				1 thru 3	B
		Test					1.0	1 thru 22	
		Replace		1.0				1 thru 3	
		Repair					2.0	1 thru 22	
011903	Oscillator and Oven Assembly, 1A1A18A1	Test		0.5				1 thru 3	B
		Test					1.0	1 thru 22	
		Replace		1.0				1 thru 3	
		Repair					2.0	1 thru 22	
01190301	Oscillator and Oven Subassembly, A1A18A1A1	Test					0.5	1 thru 22	
		Repair					0.5	1 thru 22	
01190302	Oscillator and Oven Subassembly, 1A1A18A1A2	Test					0.5	1 thru 22	
		Repair					0.5	1 thru 22	
0120	Modem Subassembly MX-7373/G, 1A1A19	Inspect		0.3					
		Test		0.5				1 thru 3	A
		Test				1.0		1 thru 14	
		Adjust				1.0		1 thru 14	
		Replace		0.3				1 thru 3	
		Repair				2.0		1 thru 14	
012001	Electrical Component Assembly, 1A1A19TB1	Test				0.5		1 thru 14	B
		Test					1.0	1 thru 22	
		Replace				1.0		1 thru 14	
		Repair					2.0	1 thru 22	

SECTION II MAINTENANCE ALLOCATION CHART
FOR
MODEM, LOW SPEED WIRE LINE MD-674(P)/G

(1)	(2)	(3)	(4) MAINTENANCE CATEGORY					(5)	(6)
GROUP NUMBER	COMPONENT/ ASSEMBLY	MAINT. FUNCTION	C	O	F	H	D	TOOLS AND EQUIP	REMARKS
012002	Modem Subassembly, 1A1A19A2	Test		0.5				1 thru 3	B
		Test					1.0	1 thru 22	
		Replace		1.0				1 thru 3	
		Repair					2.0	1 thru 22	
012003	Oscillator and Oven Assembly, A1A1A19A1	Test		0.5				1 thru 3	B
		Test					1.0	1 thru 22	
		Replace		1.0				1 thru 3	
		Repair					2.0	1 thru 22	
01200301	Oscillator Oven Subassembly, 1A1A19A1A1	Test					0.5	1 thru 22	
		Repair					0.5	1 thru 22	
01200302	Oscillator and Oven Subassembly. 1A1A9A1A2	Test					0.5	1 thru 22	
		Repair					0.5	1 thru 22	
0121	Modem Subassembly MX-7374/C, 1A1A20	Inspect		0.3					
		Test		0.5				1 thru 3	A
		Test				1.0		1 thru 14	
		Adjust				1.0		1 thru 14	
		Replace		0.3				1 thru 3	
		Repair				2.0		1 thru 14	
012101	Electrical Component Assembly. 1A1A20TB1	Test				0.5		1 thru 14	B
		Test					1.0	1 thru 22	
		Replace				1.0		1 thru 14	
		Repair					2.0	1 thru 22	
012102	Modem Subassembly, 1A1A20A2	Test		0.5				1 thru 3	B
		Test					1.0	1 thru 22	
		Replace		1.0				1 thru 3	
		Repair					2.0	1 thru 22	
012103	Oscillator and Oven Assembly, 1A1A20A1	Test		0.5				1 thru 3	B
		Test					1.0	1 thru 22	
		Replace		1.0				1 thru 3	
		Repair					2.0	1 thru 22	
01210301	Oscillator Oven Subassembly, 1A1A20A1A1	Test					0.5	1 thru 22	
		Repair					0.5	1 thru 22	
01210302	Oscillator and Oven Subassembly, 1A1A20A1A2	Test					0.5	1 thru 22	
		Repair					0.5	1 thru 22	
0122	Modem Subassembly MX-7375/C, 1A1A21	Inspect		0.3					
		Test		0.5				1 thru 3	A
		Test				1.0		1 thru 14	
		Adjust				1.0		1 thru 14	
		Replace		0.3				1 thru 3	
		Repair				2.0		1 thru 14	
012201	Electrical Component Assembly, 1A1A21TB1	Test				0.5		1 thru 14	B
		Test					1.0	1 thru 22	
		Replace				1.0		1 thru 14	
		Repair					2.0	1 thru 22	
012202	Modem Subassembly, 1A1A21A2	Test		0.5				1 thru 3	B
		Test					1.0	1 thru 22	
		Replace		1.0				1 thru 3	
		Repair					2.0	1 thru 22	
012203	Oscillator and Oven Assembly, 1A1A21A1	Test		0.5				1 thru 3	B
		Test					1.0	1 thru 22	
		Replace		1.0				1 thru 3	
		Repair					2.0	1 thru 22	
01220301	Oscillator Oven Subassembly, 1A1A21A1A1	Test					0.5	1 thru 22	
		Repair					0.5	1 thru 22	
01220302	Oscillator and Oven Subassembly, 1A1A21A1A2	Test					0 5	1 thru 22	
		Repair					0.5	1 thru 22	

SECTION II MAINTENANCE ALLOCATION CHART
FOR
MODEM, LOW SPEED WIRE LINE MD-674(P)/G

(1)	(2)	(3)	(4) MAINTENANCE CATEGORY					(5)	(6)
GROUP NUMBER	COMPONENT/ ASSEMBLY	MAINT. FUNCTION	C	O	F	H	D	TOOLS AND EQUIP	REMARKS
0123	Modem Subassembly MX-7376/G, 1A1A22	Inspect		0.3					
		Test		0.5				1 thru 3	A
		Test				1.0		1 thru 14	
		Adjust				1.0		1 thru 14	
		Replace		0.3				1 thru 3	
		Repair				2.0		1 thru 14	
012301	Electrical Component Assembly, 1A1A22TB1	Test				0.5		1 thru 14	B
		Test					1.0	1 thru 22	
		Replace				1.0		1 thru 14	
		Repair					2.0	1 thru 22	
012302	Modem Subassembly, 1A1A22A2	Test		0.5				1 thru 3	B
		Test					1.0	1 thru 22	
		Replace		1.0				1 thru 3	
		Repair					2.0	1 thru 22	
012303	Oscillator and Oven Assembly, 1A1A22A1	Test		0.5				1 thru 3	B
		Test					1.0	1 thru 22	
		Replace		1.0				1 thru 3	
		Repair					2.0	1 thru 22	
01230301	Oscillator Oven Subassembly, 1A1A22A1A1	Test					0.5	1 thru 22	
		Repair					0.5	1 thru 22	
01230302	Oscillator and Oven Subassembly, 1A1A22A1A2	Test					0.5	1 thru 22	
		Repair					0.5	1 thru 22	
0124	Modem Subassembly MX-7377/G, 1A1A23	Inspect		0.3					
		Test		0.5				1 thru 3	A
		Test				1.0		1 thru 14	
		Adjust				1.0		1 thru 14	
		Replace		0.3				1 thru 3	
		Repair				2.0		1 thru 14	
012401	Electrical Component Assembly, 1A1A23TB1	Test				0.5		1 thru 14	B
		Test					1.0	1 thru 22	
		Replace				1.0		1 thru 14	
		Repair					2.0	1 thru 22	
012402	Modem Subassembly, 1A1A23A2	Test		0.5				1 thru 3	B
		Test					1.0	1 thru 22	
		Replace		1.0				1 thru 3	
		Repair					2.0	1 thru 22	
012403	Oscillator and Oven Assembly, 1A1A23A1	Test		0.5				1 thru 3	B
		Test					1.0	1 thru 22	
		Replace		1.0				1 thru 3	
		Repair					2.0	1 thru 22	
01240301	Oscillator and Oven Subassembly, 1A1A23A1A2	Test					0.5	1 thru 22	
		Repair					0.5	1 thru 22	
01240302	Oscillator Oven Subassembly, 1A1A23A1A1	Test					0.5	1 thru 22	
		Repair					0.5	1 thru 22	
0125	Modem Subassembly MX-7378/G, 1A1A24	Inspect		0.3					
		Test		0.5				1 thru 3	A
		Test				1.0		1 thru 14	
		Adjust				1.0		1 thru 14	
		Replace		0.3					
		Repair				2.0		1 thru 14	
012501	Electrical Component Assembly, 1A1A24TB1	Test				0.5		1 thru 14	B
		Test					1.0	1 thru 22	
		Replace				1.0		1 thru 14	
		Repair					2.0	1 thru 22	
012502	Modem Subassembly, 1A1A24A2	Test		0.5				1 thru 3	B
		Test					1.0	1 thru 22	
		Replace		1.0				1 thru 3	
		Repair					2.0	1 thru 22	
012503	Oscillator and Oven Assembly 1A1A24A1	Test		0.5				1 thru 3	B
		Test					1.0	1 thru 22	
		Replace		1.0				1 thru 3	
		Repair					2.0	1 thru 22	

SECTION II MAINTENANCE ALLOCATION CHART
FOR
MODEM, LOW SPEED WIRE LINE MD-674(P)/G

(1) GROUP NUMBER	(2) COMPONENT/ ASSEMBLY	(3) MAINT. FUNCTION	(4) MAINTENANCE CATEGORY C	O	F	H	D	(5) TOOLS AND EQUIP	(6) REMARKS
01250301	Oscillator Oven Subassembly, 1A1A24A1A1	Test					0.5	1 thru 22	
		Repair					0.5	1 thru 22	
01250302	Oscillator and Oven Subassembly, 1A1A24A1A2	Test					0.5	1 thru 22	
		Repair					0.5	1 thru 22	
0126	Modem Subassembly MX-7379/G, 1A1A25	Inspect		0.3					
		Test		0.5				1 thru 3	
		Test				1.0		1 thru 14	
		Adjust				1.0		1 thru 14	
		Replace		0.3				1 thru 3	
		Repair				2.0		1 thru 14	
012601	Electrical Component Assembly, 1A1A25TB1	Test				0.5		1 thru 14	
		Test					1.0	1 thru 22	
		Replace				1.0		1 thru 14	
		Repair					2.0	1 thru 22	
012602	Modem Subassembly, 1A1A25A3	Test		0.5				1 thru 3	
		Test					1.0	1 thru 22	
		Replace		1.0				1 thru 3	
		Repair					2.0	1 thru 22	
012603	Modem Subassembly, 1A1A25A2	Test		0.5				1 thru 3	
		Test					1.0	1 thru 22	
		Replace		1.0				1 thru 3	
		Repair					2.0	1 thru 22	
012604	Oscillator and Oven Assembly, 1A1A25A1	Test		0.5				1 thru 3	
		Test					1.0	1 thru 22	
		Replace		1.0				1 thru 3	
		Repair					2.0	1 thru 22	
01260401	Oscillator Oven Subassembly, 1A1A25A1A1	Test					0.5	1 thru 22	
		Repair					0.5	1 thru 22	
01260402	Oscillator and Oven Subassembly 1A1A25A1A2	Test					0.5	1 thru 22	
		Repair					0.5	1 thru 22	
0127	Modem Subassembly MX-7380/G, 1A1A26	Inspect		0.3					
		Test		0.5				1 thru 3	A
		Test				1.0		1 thru 14	
		Adjust				1.0		1 thru 14	
		Replace		0.3				1 thru 3	
		Repair				2.0		1 thru 14	
012701	Electrical Component Assembly, 1A1A26TB1	Test				0.5		1 thru 14	B
		Test					1.0	1 thru 22	
		Replace				1.0		1 thru 14	
		Repair					2.0	1 thru 22	
012702	Modem Subassembly, 1A1A26A2	Test		0.5				1 thru 3	B
		Test					1.0	1 thru 22	
		Replace		1.0				1 thru 3	
		Repair					2.0	1 thru 22	
012703	Oscillator and Oven Assembly, 1A1A26A1	Test		0.5				1 thru 3	B
		Test					1.0	1 thru 22	
		Replace		1.0				1 thru 3	
		Repair					2.0	1 thru 22	
01270301	Oscillator Oven Subassembly, 1A1A26A1A1	Test					0.5	1 thru 22	
		Repair					0.5	1 thru 22	
01270302	Oscillator and Oven Subassembly, 1A1A26A1A2	Test					0.5	1 thru 22	
		Repair					0.5	1 thru 22	
0128	Modem Subassembly MX-7381/G, 1A1A27	Inspect		0.3					
		Test		0.5				1 thru 3	A
		Test				1.0		1 thru 14	
		Adjust				1.0		1 thru 14	
		Replace		0.3				1 thru 3	
		Repair				2.0		1 thru 14	

SECTION II MAINTENANCE ALLOCATION CHART
FOR
MODEM, LOW SPEED WIRE LINE MD-674(P)/G

(1)	(2)	(3)	(4) MAINTENANCE CATEGORY					(5)	(6)
GROUP NUMBER	COMPONENT/ ASSEMBLY	MAINT. FUNCTION	C	O	F	H	D	TOOLS AND EQUIP	REMARKS
012801	Electrical Component Assembly, 1A1A27TB1	Test				0.5		1 thru 14	B
		Test					1.0	1 thru 22	
		Replace				1.0		1 thru 14	
		Repair					2.0		
012802	Modem Subassembly, 1A1A27A2	Test		0.5				1 thru 3	B
		Test					1.0	1 thru 22	
		Replace		1.0				1 thru 3	
		Repair					2.0	1 thru 22	
012803	Oscillator and Oven Assembly, 1A1A27A1	Test		0.5				1 thru 3	B
		Test					1.0	1 thru 22	
		Replace		1.0				1 thru 3	
		Repair					2.0	1 thru 22	
01280301	Oscillator Oven Subassembly, 1A1A27A1A1	Test					0.5	1 thru 22	
		Repair					0.5	1 thru 22	
01280302	Oscillator and Oven Subassembly, 1A1A27A1A2	Test					0.5	1 thru 22	
		Repair					0.5	1 thru 22	
0129	Modem Subassembly MX-7382/G, 1A1A28	Inspect		0.3					
		Test		0.5				1 thru 3	A
		Test				1.0		1 thru 14	
		Adjust				1.0		1 thru 14	
		Replace		0.3				1 thru 3	
		Repair				2.0		1 thru 14	
012901	Electrical Component Assembly, 1A1A28TB1	Test				0.5		1 thru 14	B
		Test					1.0	1 thru 22	
		Replace				1.0		1 thru 14	
		Repair					2.0	1 thru 22	
012902	Modem Subassembly, 1A1A28A2	Test		0.5				1 thru 3	B
		Test					1.0	1 thru 22	
		Replace		1.0				1 thru 3	
		Repair					2.0	1 thru 22	
012903	Oscillator and Oven Assembly, 1A1A28A1	Test		0.5				1 thru 3	B
		Test					1.0	1 thru 22	
		Replace		1.0				1 thru 3	
		Repair					2.0	1 thru 22	
01290301	Oscillator and Oven Subassembly, 1A1A28A1A2	Test					0.5	1 thru 22	
		Repair					0.5	1 thru 22	
01290302	Oscillator Oven Subassembly, 1A1A28A1A1	Test					0.5	1 thru 22	
		Repair					0.5	1 thru 22	
0130	Modem Subassembly MX-7383/G, 1A1A29	Inspect		0.3					
		Test		0.5				1 thru 3	A
		Test				1.0		1 thru 14	
		Adjust				1.0		1 thru 14	
		Replace		0.3				1 thru 3	
		Repair				2.0		1 thru 14	
013001	Electrical Component Assembly, 1A1A29TB1	Test				0.5		1 thru 14	B
		Test					1.0	1 thru 22	
		Replace				1.0		1 thru 14	
		Repair					2.0	1 thru 22	
013002	Modem Subassembly, 1A1A29A2	Test		0.5				1 thru 3	B
		Test					1.0	1 thru 22	
		Replace		1.0				1 thru 3	
		Repair					1.0	1 thru 22	
013003	Oscillator and Oven Assembly, 1A1A29A1	Test		0.5				1 thru 3	B
		Test					1.0	1 thru 22	
		Replace		1.0				1 thru 3	
		Repair					2.0	1 thru 22	
01300301	Oscillator Oven Subassembly, 1A1A29A1A1	Test					0.5	1 thru 22	
		Repair					0.5	1 thru 22	
01300302	Oscillator and Oven Subassembly, 1A1A29A1A2	Test					0.5	1 thru 22	
		Repair					0.5	1 thru 22	

SECTION II MAINTENANCE ALLOCATION CHART
FOR
MODEM, LOW SPEED WIRE LINE MD-674(P)/G

(1)	(2)	(3)	(4) MAINTENANCE CATEGORY					(5)	(6)
GROUP NUMBER	COMPONENT/ ASSEMBLY	MAINT. FUNCTION	C	O	F	H	D	TOOLS AND EQUIP	REMARKS
0131	Modem Subassembly MX-7384/G, 1A1A30	Inspect		0.3					
		Test		0.5				1 thru 3	A
		Test				1.0		1 thru 14	
		Adjust				1.0		1 thru 14	
		Replace		0.3				1 thru 3	
		Repair				2.0		1 thru 14	
013101	Electrical Component Assembly, 1A1A30TB1	Test				0.5		1 thru 14	B
		Test					1.0	1 thru 22	
		Replace				1.0		1 thru 14	
		Repair					2.0	1 thru 22	
013102	Oscillator and Oven Assembly, 1A1A30A1	Test		0.5				1 thru 3	B
		Test					1.0	1 thru 22	
		Replace		1.0				1 thru 3	
		Repair					2.0	1 thru 22	
01310201	Oscillator and Oven Subassembly, 1A1A30A1A2	Test					0.5	1 thru 22	
		Repair					0.5	1 thru 22	
01310202	Oscillator Oven Subassembly, 1A1A30A1A1	Test					0.5	1 thru 22	
		Repair					0.5	1 thru 22	
0132	Modem Subassembly MX-7385/G, 1A1A31	Inspect		0.3					
		Test		0.5				1 thru 3	A
		Test				1.0		1 thru 14	
		Adjust				1.0		1 thru 14	
		Replace		0.3				1 thru 3	
		Repair				2.0		1 thru 14	
013201	Electrical Component Assembly, 1A1A31TB1	Test				0.5		1 thru 14	B
		Test					1.0	1 thru 22	
		Replace				1.0		1 thru 14	
		Repair					2.0	1 thru 22	
013202	Oscillator and Oven Assembly, 1A1A31A1	Test		0.5				1 thru 3	B
		Test					1.0	1 thru 22	
		Replace		1.0				1 thru 3	
		Repair					2.0	1 thru 22	
01320201	Oscillator Oven Subassembly, 1A1A31A1A1	Test					0.5	1 thru 22	
		Repair					0.5	1 thru 22	
01320202	Oscillator and Oven Subassembly, 1A1A31A1A2	Test					0.5	1 thru 22	
		Repair					0.5	1 thru 22	
0133	Modem Subassembly MX-7386/G, 1A1A32	Inspect		0.3					
		Test		0.5				1 thru 3	A
		Test				1.0		1 thru 14	
		Adjust				1.0		1 thru 14	
		Replace		0.3				1 thru 3	
		Repair				2.0		1 thru 14	
013301	Electrical Component Assembly, 1A1A32TB1	Test				0.5		1 thru 14	B
		Test					1.0	1 thru 22	
		Replace				1.0		1 thru 14	
		Repair					2.0	1 thru 22	
013302	Oscillator and Oven Assembly, 1A1A32A1	Test		0.5				1 thru 3	B
		Test					1.0	1 thru 22	
		Replace		1.0				1 thru 3	
		Repair					2.0	1 thru 22	
01330201	Oscillator Oven Subassembly, 1A1A32A1A1	Test					0.5	1 thru 22	
		Repair					0.5	1 thru 22	
01330202	Oscillator and Oven Subassembly, 1A1A32A1A2	Test					0.5	1 thru 22	
		Repair					0.5	1 thru 22	
02	Case, Electrical Equipment 1A2	Inspect		0.2					
		Test		0.5				1 thru 3	
		Repair			1.0			1,2,5	

SECTION III TOOL AND TEST EQUIPMENT REQUIREMENTS FOR MODEM, LOW SPEED WIRE LINE MD-674(P)/G

TOOL OR TEST EQUIPMENT REF CODE	MAINTENANCE CATEGORY	NOMENCLATURE	NATIONAL/NATO STOCK NUMBER	TOOL NUMBER
1	O, F, H, D	MULTIMETER AN/USM-223	6625-00-999-7465	
2	O, F, H, D	OSCILLOSCOPE AN/USM-281C	6625-00-106-9622	
3	O, F, H, D	TOOL KIT, ELECTRONIC EQUIPMENT TK-101/G	5180-00-064-5178	
4	F, H, D	TOOK KIT, ELECTRONIC EQUIPMENT TK-100/G	5180-00-605-0079	
5	F, H, D	TOOL KIT, ELECTRONIC EQUIPMENT TK-105/G	5180-00-610-8177	
6	F, H, D	EXTENDER CARD D80034010 (P/O MD-674(P)/G)	5805-00-926-7313	
7	F, H, D	VOLTMETER ME-303A/U	6625-00-421-7352	
8	F, H, D	TEST SET, SEMICONDUCTOR DEVICE TS-1836C/U	6625-00-159-2263	
9	F, H, D	POWER SUPPLY PP-6921/U	6625-00-051-5896	
10	F, H, D	VOLTMETER, ELCETRONIC ME-429/U	6625-00-229-0457	
11	H, D	COUNTER, ELECTONIC, DIGITAL CP-772 A/U	6625-00-973-4387	
12	H, D	ATTENUATOR ASSEMBLY CN-1000/U	6625-00-215-4931	
13	H, D	TEST SET TELEGRAPH AN/GGM-15(V)1	6625-00-464-1702	
14	H, D	TEMPERATURE TESTER (SIMPSON MODEL 388-3L)	6685-00-975-4544	
15	D	LINE AMPLIFIER STELMA LA-1	7440-00-933-9972	
16	D	STOPWATCH	6645-00-719-8670	
17	D	VARIABLE FREQUENCY POWER SOURCE CML N1500A/SG-13A	6130-00-008-3939	
18	D	CAPACITOR DECADE AN/URM-2	6625-00-405-6430	
19	D	PULSE GENERATOR SET AN/UPM-15A	6625-00-682-2581	
20	D	WIDE RANGE OSCILLATOR 0-1025/U	6625-00-518-4659	
21	D	AUTOTRNFORMER 110/220 VAC 500 VA		
22	D	MODEM, LOW SPEED WIRE LINE MD-674(P)/G	5805-00-985-9179	
		NOTE: Equivalent (Replacement) test equipment may be substituted for the above.		

SECTION IV. REMARKS

REFERENCE CODE	REMARKS
A	Organizational maintenance will be performed by and at Direct Support, Organizational test is limited to equipment operation, and those tests using the limited test equipment indicated in the TOOL AND TEST EQUIPMENT REQUIREMENTS. Organizational repair is limited to external parts and replacement of indicated subassemblies.
B	Test and replace assembly and/or subassembly as indicated. Repair will be performed at depot level.

APPENDIX C

COMPONENTS OF END ITEM LIST

SECTION I. INTRODUCTION

C-1. SCOPE

This appendix lists components of end item and basic issue items for the (insert short item name) to help you inventory items required for safe and efficient operation.

C-2. GENERAL

Components of End Item. This listing is for informational purposes only, and is not authority to requisition replacements. These items are part of the end item, but are removed and separately packaged for transportation or shipment. As part of the end item, these items must be with the end item whenever it is used or transferred between property accounts. Illustrations are furnished to assist you in identifying the items.

C-3. EXPLANATION OF COLUMNS

The following provides an explanation of columns found in the tabular listings:

a. Column (1) - National Stock Number. Indicates the National stock number assigned to the item and will be used for requisitioning purposes.

b. Column (2) - Descriptor Indicates the Federal item name and, if required, a minimum description to identify and locate the item. The last line for each item indicates the FSCM (in parentheses) followed by the part number.

c. Column (3) - Unit of Measure (U/M). Indicates the measure used in performing the actual operational/ maintenance function. This measure is expressed by a two-character alphabetical abbreviation (e.g., ea, in, pr).

d. Column (4) - Quantity required (Qty rqr). Indicates the quantity of the item authorized to be used with/on the equipment.

SECTION II. COMPONENTS OF END ITEM

(1) National Stock Number	(2) Description, Part Number and FSCM	(3) U/M	(4) Qty rqr
	NOTE The part number is followed by the applicable five digit Federal supply code for manufacturers or distributor or Government agency, etc., which is identified in SB 708-42.		
	Chassis, Electrical Equipment: over-all dimensions 12.000 inches by 17.750 inches by 19.000 inches; part number D90034003; 96238 (installed in equipment)		
5805-00-916-9627	Modem Subassembly: voice control oscillator: 80034090-000; 96238 (installed in equipment)	EA	1
5805-00-916-9628	Modem Subassembly: 128 divider "A": 80034100-000; 96238 (installed in equipment)	EA	1
5805-00-933-2839	Modem Subassembly: add/subtract and talk request generator: 80034140-000; 96238 (installed in equipment)	EA	1
5805-00-916-9641	Modem Subassembly: 128 divider "B": 80034080-000; 96238 (installed in equipment)	EA	1
5805-00-916-9635	Modem Subassembly: dual output polar divider: 80034150-000; 96238 (installed in equipment)	EA	1
5805-00-933-2516	Modem Subassembly: transmit output carrier alarm: 80034120-000; 96238 (installed in equipment)	EA	1
5805-00-916-9640	Modem Subassembly: 64 divider: 80034130-000; 96238 (installed in equipment)	EA	1
5805-00-933-4028	Modem Subassembly: demodulator: 80034020-000; 96238 (installed in equipment)	EA	1
5805-00-916-9625	Modem Subassembly: receive carrier alarm: 80034050-000; 96238 (installed in equipment)	EA	1
5805-00-916-9624	Modem Subassembly: talk request signal detector: 80034040-000; 96238 (installed in equipment)	EA	1
5805-00-916-9623	Modem Subassembly: data output: 80034030-000; 96238 (installed in equipment)	EA	1
5805-00-916-9642	Modem Subassembly: input interface and alarm circuit: 80034060-000; 96238 (installed in equipment)	EA	1
5805-00-926-7313	Modem Subassembly: adapter: 80034010-000; 96238 (installed in equipment)	EA	1
5805-00-933-4027	Modem Subassembly: power supply regulator, plus or minus 15 volt: 80034160-000; 96238 (installed in equipment)	EA	1
5805-00-916-9633	Modem Subassembly: power supply regulator, plus or minus 15 volt: 80034170-000; 96238 (installed in equipment)	EA	1
	NOTE The following item is to be issued only when the end item is used as part of a sub-terminal.		
5805-00-920-7159	Clock Module Group-OA-8072CG: 80058	EA	1
	NOTE Only one of the following modem subassemblies is to be issued with each end item depending on frequency operation.		
5805-00-926-2628	Modem Subassembly-MX-7372/G: 90034005-001; 96238	EA	1
	OR		
5805-00-926-2629	Modem Subassembly-MX-7373/G: 90034005-002; 96238	EA	1
	OR		
5805-00-926-2630	Modem Subassembly-MX-7374/G: 90034005-003; 96238	EA	1
	OR		
5805-00-926-2597	Modem Subassembly-MX-7375/G: 90034005-004; 96238	EA	I
	OR		
5805-00-926-2598	Modem Subassembly-MX-7376/G: 90034005-005; 96238	EA	1
	OR		
5805-00-926-2631	Modem Subassembly-MX-7377/G: 90034005-006; 96238	EA	1
	OR		
5805-00-926-2612	Modem Subassembly-MX-7378/G: 900.34005-007; 96238	EA	1
	OR		
5805-00-933-2515	Modem Subassembly-MX-7379/U: 90034005-082; 96238	EA	1
	OR		
5805-00-926-2614	Modem Subassembly-MX-7380/G: D90034005-009; 96238	EA	1
	OR		
5805-00-926-2600	Modem Subassembly-MX-7381/G: D90034005-018; 96238	EA	1
	OR		
5805-00-926-2632	Modem Subassembly-MX-7382/G: 90034005-011; 96238	EA	1
	OR		
5805-00-926-2633	Modem Subassembly-MX-7383/G: 90034005-012; 96238	EA	1
	OR		
5805-00-926-2613	Modem Subassembly-MX-7384/G: 90034005-013; 96238	EA	1
	OR		
5805-00-926-2615	Modem Subassembly-MX-7385/G: 90034005-014; 96238	EA	1
	OR		
5805-00-926-2603	Modem Subassembly-MX-7386/G: 90034005-015; 96238	EA	1

SECTION II. COMPONENTS OF END ITEM

(1) National Stock Number	(2) Description, Part Number and FSCM	(3) U/M	(4) Qty rqr
	CHASSIS ELECTRICAL EQUIPMENT		
	Fuse, Cartridge: :3 amp: GBA3; 71400 (installed equipment)	EA	1
	CLOCK MODULE GROUP-OA-8072/G		
5805-00-916-9626	Clock Module Group Subassembly: 8 divider clock module: 80034110-000; 96238	EA	1
5963-00-933-3664	Oscillator, Radio Frequency: provides all the necessary timing for control phasing data regeneration, and timing for associated terminal equipment: 1.228800 megacycles frequency: 48075004-000; 96238	EA	
	MODEM SUBASSEMBLY-MX-7372/G		
5915-00-915-8933	Filter, Bandpass: 425 to 595 cycles per second bandwidth: 510 cycles per second operating frequency: 1000 ohms input, 600 ohms output impedance: A43020016-001; 96238	EA	1
5915-00-918-7888	Filter, Bandpass: 425 to 595 cycles per second bandwidth: 510 cycles per second operating frequency: 600 ohms input, 5000 ohms output impedance; A43020017-001; 96238	EA	1
5915-00-916-6088	Network, Phase Changing: 510 cycles per second operating frequency: 43006003-001; 96238	EA	1
5805-00-916-6026	Oscillator and Oven Assembly: 425 cycles per second mark frequency, 595 cycles per second space frequency: 90034007-001; 96238	EA	1
5955-00-933-8674	Crystal Unit, Quartz: 217.600 KC, nominal fundamental frequency: A40040012-012; 96238	EA	1
5955-00-937-0420	Crystal Unit, Quartz: 304.640 KC, nominal fundamental frequency: A40040012-020: 96238	EA	1
5805-00-916-9630	Modem Subassembly: frequency determining 8 divider: SM-D-581194; 80063	EA	1
	OR		
	MODEM SUBASSEMBLY-MX-7373/G		
5915-00-926-8122	Filter, Bandpass: 510 to 850 cycles per second bandwidth: 680 cycles per second operating frequency: 1000 ohms input, 600 ohms output impedance: 43020016-002; 96238	EA	I
5915-00-926-8095	Filter, Bandpass: 510 to 850 cycles per second bandwidth: 680 cycles per second operating frequency: 600 ohms input, 5000 ohms output impedance: A43020017-002; 96238	EA	1
5915-00-916-6089	Network, Phase Changing: 680 cycles per second operating frequency: 43006003-002; 96238	EA	1
5805-00-916-6025	Oscillator and Oven Assembly: 510 cycles per second mark frequency, 850 cycles per second space frequency: 90034007-002; 96238	EA	1
5955-00-933-8675	Crystal Unit, Quartz: 261.120 KC, nominal fundamental frequency: 40040012-016; 96238	EA	1
5955-00-968-6199	Crystal Unit, Quartz: 435.200 KC, nominal fundamental frequency: 40040012-024; 96238	EA	1
5805-00-916-9630	Modem Subassembly: frequency determining 8 divider: SM-D-581194; 80063	EA	1
	OR		
	MODEM SUBASSEMBLY-MX-7374/G		
5915-00-914-8932	Filter, Bandpass: 765 cycles per second to 935 cycles per second bandwidth, 850 cycles per second operating frequency: 1000 ohms input, 600 ohms output impedance: 43020016-003; 96238	EA	1
5915-00-918-7944	Filter, Bandpass: 765 cycles per second to 935 cycles per second bandwidth, 850 cycles per second operating frequency: 600 ohms input, 5000 ohms output impedance: 43020017-003; 96238	EA	1
5915-00-916-6090	Network, Phase Changing: 850 cycles per second operating frequency: 43006003-003; 96238	EA	1
5805-00-916-6024	Oscillator and Oven Assembly: 765 cycles per second mark frequency, 935 cycles per second space frequency: 90034007-003; 96238	EA	1
5955-00-933-8671	Crystal Unit, Quartz: 195.840 KC, nominal fundamental frequency: 40040012-010; 96238	EA	1
5955-00-973-1456	Crystal Unit, Quartz: 239.360 KC, nominal fundamental frequency: A40040012-014; 96238	EA	1
5805-00-916-9631	Modem Subassembly: frequency determining 4 divider: 80034190-000; 96238	EA	1

SECTION II. COMPONENTS OF END ITEM

(1) National Stock Number	(2) Description, Part Number and FSCM	(3) U/M	(4) Qty rqr
	OR		
	MODEM SUBASSEMBLY-MX-7375/G		
5915-00-914-8916	Filter Bandpass: 680 cycles per second to 1.360 KC bandwidth, 1.020 KC operating frequency; 1000 ohms input, 600 ohms output impedance: 43020016-004; 96238	EA	1
5915-00-918-7946	Filter, Bandpass: 680 cycles per second to 1.360 KC bandwidth, 1.020 KC operating frequency: 600 ohms input, 5000 ohm output impedance: 43020017-004; 96238	EA	1
5915-00-916-6091	Network, Phase Changing: 1.020 KC, operating frequency: 43006003-004; 96238	EA	1
5805-00-916-6023	Oscillator and Oven Assembly: 680 cycles per second mark frequency, 1.360 KC space frequency: 90034007-004; 96238	EA	1
5955-00-937-0421	Crystal Unit, Quartz: 174.080 KC, nominal fundamental frequency: A40040012-006; 96238	EA	1
5955-00-968-6385	Crystal Unit, Quartz: 348.160 KC, nominal fundamental frequency: A40040012-23; 96238	EA	1
5805-00-916-9631	Modem Subassembly: frequency determining 4 divider: 80034190-000; 96238	EA	1
	OR		
	MODEM SUBASSEMBLY-MX-7376/G		
5915-00-914-8871	Filter, Bandpass: 1.105 to 1.275 KC bandwidth: 1.190 KC, operating frequency: 1000 ohms input, 600 ohms output impedance: 43020016-005; 96238	EA	1
5915-00-918-7952	Filter, Bandpass: 1.105 to 1.275 KC bandwidth: 1.190 KC, operating frequency: 600 ohms input, 5000 ohms output impedance: A43020017-005; 96238	EA	1
5915-00-916-6092	Network, Phase Changing: 1.190 KC, operating frequency: 43006003-005; 96238	EA	1
5805-00-916-6037	Oscillator and Oven Assembly: 1.105 KC mark frequency, 1.275 KC space frequency: 90034007-005; 96238	EA	1
5955-00-933-7732	Crystal Unit, Quartz: 282.880 KC, nominal fundamental frequency: 40040012-18; 96238	EA	1
5955-00-983-7170	Crystal Unit, Quartz: 326.400 KC, nominal fundamental frequency: A40040012-022; 96238	EA	1
5805-00-916-9631	Modem Subassembly: frequency determining 4 divider: 80034190-000; 96238	EA	1
	OR		
	MODEM SUBASSEMBLY-MX-7377/G		
5915-00-914-8851	Filter, Bandpass: 1.190 to 1.530 KC bandwidth: 1.360 KC, operating frequency: 1000 ohms input, 600 ohms output impedance: 43020016-006; 96238	EA	1
5915-00-918-7953	Filter, Bandpass: 1.190 to 1.530 KC bandwidth: 1.360 KC, operating frequency: 600 ohms input, 5000 ohms output impedance: 43020017-006; 96238	EA	1
5915-00-916-6093	Network, Phase Changing: 1.360 KC, operating frequency: 43006003-006; 96238	EA	I
5805-00-916-6036	Oscillator and Oven Assembly: 1.190 KC mark frequency, 1.530 KC space frequency: 90034007-006; 96238	EA	1
5955-00-933-9332	Crystal Unit, Quartz: 152.320 KC, nominal fundamental frequency: A40040012-001; 96238	EA	1
5955-00-933-8671	Crystal Unit Quartz: 195.840 KC, nominal fundamental frequency: 40040012-010; 96238	EA	1
5805-00-916-9632	Modem Subassembly: frequency determining 2 divider: 80034180-000; 96238	EA	1
	OR		
	MODEM SUBASSEMBLY-MX-7378/G		
5915-00-914-8847	Filter, Bandpass: 1.445 to 1.615 KC bandwidth: 1.530 KC, operating frequency: 1000 ohms input, 600 ohms output impedance: 43020016-007; 96238	EA	1
5915-00-918-7956	Filter Bandpass: 1.445 to 1.615 KC bandwidth: 1.530 KC, operating frequency: 600 ohms input, 5000 ohms output impedance: 43020017-007; 96238	EA	1
5915-00-916-6094	Network, Phase Changing: 1.530 KC, operating frequency: 43006003-007; 96238	EA	1
5805-00-916-6035	Oscillator and Oven Assembly: 1.445 KC mark frequency, 1.615 KC space frequency: 90034007-007; 96238	EA	1
5955-00-933-8669	Crystal Unit, Quartz: 184.960 KC, nominal fundamental frequency: A40040012-008; 96238	EA	1
5955-00-t'33-8673	Crystal Unit Quartz: 206.720 KC, nominal fundamental frequency: A40040012-011; 96238	EA	1
5805-00-916-9632	Modem Subassembly: frequency determining 2 divider: 80034180-000; 96238	EA	I

SECTION II. COMPONENTS OF END ITEM

(1) National Stock Number	(2) Description, Part Number and FSCM	(3) U/M	(4) Qty rqr
	OR		
	MODEM SUBASSEMBLY-MX-7379/G		
5915-00-918-7881	Filter, Bandpass: 1.200 to 2.400 KC bandwidth: 1.800 KC, operating frequency: 1000 ohms input, 600 ohms output impedance; 43020016-008: 96238	EA	1
5915-00-918-7957	Filter, Bandpass: 1.200 to 2.400 KC bandwidth: 1.800 KC, operating frequency: 600 ohms input, 5000 ohms output impedance: 43020017-008; 96238	EA	1
5915-00-916-6095	Network, Phase Changing: 1.800 KC operating frequency: 43006003-008; 96238	EA	1
5805-00-916-6018	Oscillator and Oven Assembly: 1.200 KC mark frequency, 2.400 KC space frequency: 90034007-008; 96238	EA	1
5955-00-973-1440	Crystal Unit, Quartz: 153.600 KC, nominal fundamental frequency: 400400112-002; 96238	EA	1
	Crystal Unit, Quartz: 307.200 KC, nominal fundamental frequency: 40040012-021: 96238	EA	1
5805-00-916-9632	Modem Subassembly: frequency determining 2 divider: 80034180-000; 96238	EA	1
5805-00-916-9629	Modem Subassembly: delay equalizer: 80034230-000; 96238	EA	1
	OR		
	MODEM SUBASSEMBLY-MX-7380/G		
5915-00-914-6768	Filter, Bandpass: 1.785 to 1.955 KC bandwidth: 1.870 KC, operating frequency: 1000 ohms input, 600 ohms output impedance: 43020016-009; 96238	EA	1
5915-00-918-9337	Filter, Bandpass: 1.785 to 1.955 KC bandwidth: 1.870 KC, operating frequency: 600 ohms input, 5000 ohms output impedance: 430020017-009; 96238	EA	1
5915-00-916-6096	Network, Phase Changing: 1.870 KC operating frequency: 43006003-009; 96238	EA	1
5805-00-916-6017	Oscillator and Oven Assembly: 1.785 KC mark frequency, 1.955 KC space frequency: D90034007-009; 96238	EA	1
5955-00-933-9333	Crystal Unit, Quartz: 228.480 KC, nominal fundamental frequency: A40040012-013; 96238	EA	1
5955-00-933-8676	Crystal Unit, Quartz: 250.240 KC, nominal fundamental frequency: A40040012-015; 96238	EA	1
5805-00-916-9632	Modem Subassembly: frequency determining 2 divider: 80034180-000; 96238	EA	1
	OR'		
	MODEM SUBASSEMBLY-MX-7381/G		
5915-00-761-4212	Filter, Bandpass: 1.870 to 2.210 KC bandwidth: 2.040 KC, operating frequency: 1000 ohms input, 600 ohms output impedance: A43020016-010; 96238	EA	1
5915-00-918-9345	Filter Bandpass: 1.870 to 2.210 KC bandwidth: 2.040 KC operating frequency: 600 ohms input, 5000 ohms output impedance: A43020017-010; 96238	EA	1
5915-00-916-6097	Network, Phase Changing: 2.040 KC operating frequency: 43006003-010; 96238	EA	1
5805-00-917-1373	Oscillator and Oven Assembly: 1.870 KC mark frequency, 2.210 KC space frequency: D90034007-010; 96238	EA	1
5955-00-973-1456	Crystal Unit, Quartz: 239.360 KC, nominal fundamental frequency: 40040012-014; 96238	EA	1
5955-00-933-7732	Crystal Unit, Quartz: 282.880 KC, nominal fundamental frequency: A40040012-18; 96238	EA	1
5805-00-916-9632	Modem Subassembly: frequency determining 2 divider: 80034180-000; 96238	EA	1
	OR		
	MODEM SUBASSEMBLY-MX-7382/G		
5915-00-761-3496	Filter, Bandpass: 2.125 to 2.295 KC bandwidth: 2.210 KC, operating frequency: 1000 ohms input, 600 ohms output impedance: A43020016-011; 96238	EA	1
5915-00-918-9377	Filter, Bandpass: 2.125 to 2.295 KC bandwidth: 2.210 KC, operating frequency: 600 ohms input, 5000 output impedance: 43020017-011; 96238	EA	1
5915-00-916-6098	Network, Phase Changing: 2.210 KC operating frequency: A43006003-011; 96238	EA	1
5805-00-917-1374	Oscillator and Oven Assembly: 2.125 KC mark frequency, 2.295 KC space frequency: 90034007-011; 96238	EA	1
	Crystal Unit, Quartz: 272.000 KC, nominal fundamental frequency: A40040012-017; 96238	EA	1
5955-00-968-6253	Crystal Unit, Quartz: 293.760 KC, nominal fundamental frequency: A40040012-019; 96238	EA	1
5805-00-916-9632	Modem Subassembly: frequency determining 2 divider: 80034180-000; 96238	EA	1

SECTION II. COMPONENTS OF END ITEM

(1) National Stock Number	(2) Description, Part Number and FSCM	(3) U/M	(4) Qty rqr
	OR		
	MODEM SUBASSEMBLY-MX-7383/G		
5915-00-916-5967	Filter, Bandpass: 2.040 to 2.720 KC bandwidth: 2.380 KC, operating frequency: 1000 ohms input, 600 ohms output impedance: 43020016-012; 96238	EA	1
5915-00-926-8107	Filter, Bandpass: 2.040 td 2.720 KC bandwidth: 2.380 KC, operating frequency: 600 ohms input, 5000 ohms output impedance: 43020017-012; 96238	EA	1
5915-00-916-6099	Network, Phase Changing: 2.380 KC operating frequency: 43006003-012; 96238	EA	1
5805-00-916-6022	Oscillator and Oven Assembly: 2.040 KC mark frequency, 2.720 KC space frequency: 90034007-012; 96238	EA	1
5955-00-933-8675	Crystal Unit, Quartz: 261.120 KC, nominal fundamental frequency: A40040012-16; 96238	EA	1
5955-00-968-6385	Crystal Unit, Quartz: 348.160 KC, nominal fundamental frequency: A40040012-23; 96238	EA	1
5805-00-916-9632	Modem Subassembly: frequency determining 2 divider: 80034180-000; 96238	EA	1
	OR		
	MODEM SUBASSEMBLY-MX-7384/G		
5915-00-916-5966	Filter, Bandpass: 2.465 to 2.635 KC bandwidth: 2.550 KC, operating frequency: 1000 ohms input, 600 ohms output impedance: A43020016-013; 96238	EA	I
5915-00-926-8109	Filter, Bandpass: 2.465 to 2.635 KC bandwidth: 2.550 KC, operating frequency: 600 ohms input, 5000 ohms output impedance: A43020017-013; 96238	EA	1
5915-00-916-6100	Network, Phase Changing: 2.550 KC operating frequency: A43006003-013; 96238	EA	1
5805-00-917-1375	Oscillator and Oven Assembly: 2.465 KC mark frequency, 2.635 KC space frequency: D90034007-013; 96238	EA	1
5955-00-973-1392	Crystal Unit, Quartz: 157.760 KC, nominal fundamental frequency: A40040012-003; 96238	EA	1
5955-00-!374-6449	Crystal Unit, Quartz: 168.640 KC, nominal fundamental frequency: A40040012-005; 96238	EA	1
	OR		
	MODEM SUBASSEMBLY-MX-7385/G		
5915-00-916-6074	Filter, Bandpass: 2.550 to 2.890 KC bandwidth: 2.720 KC, operating frequency: 1000 ohms input, 600 ohms impedance: A43020016-014; 96238	EA	I
5915-00-926-8100	Filter, Bandpass: 2.550 to 2.890 KC bandwidth: 2.720 KC, operating frequency: 600 ohms input, 5000 output impedance: A43020017-014; 96238	EA	1
5915-00-916-6101	Network, Phase Changing: 2.720 KC operating frequency: 43006003-014; 96238	EA	1
5805-00-927-7309	Oscillator and Oven Assembly: 2.550 KC mark frequency; 2.890 KC space frequency: 90034007-014: 96238	EA	1
5955-00-974-6450	Crystal Unit, Quartz: 163.200 KC, nominal fundamental frequency: A40040012-004; 96238	EA	1
5955-00-933-8669	Crystal Unit, Quartz: 184.960 KC, nominal fundamental frequency: A40040012-008; 96238	EA	1
	OR		
	MODEM SUBASSEMBLY-MX-7386/G		
5915-00-916-6073	Filter, Bandpass: 2.805 to 2.975 KC bandwidth: 2.890 KC, operating frequency: 1000 ohms input, 600 ohms output impedance: A43020016-015; 96238	EA	1
5915-00-933-7638	Filter, Bandpass: 2.805 to 2.975 KC bandwidth: 2.890 KC, operating frequency: 600 ohms input, 5000 ohms output impedance: 43020017-015; 96238.	EA	1
5915-00-916-6102	Network, Phase Changing: 2.890 KC operating frequency: 43006003-015; 96238	EA	1
5805-00-916 6019	Oscillator and Oven Assembly: 2.805 KC mark frequency, 2.975 KC space frequency: 90034007-015; 96238	EA	1
5955-00-933-8670	Crystal Unit, Quartz: 179.520 KC, nominal fundamental frequency: A40040012-007; 96238	EA	1
5955-00-933-8672	Crystal Unit, Quartz: 190.400 KC, nominal fundamental frequency: A40040012-009; 96238	EA	I

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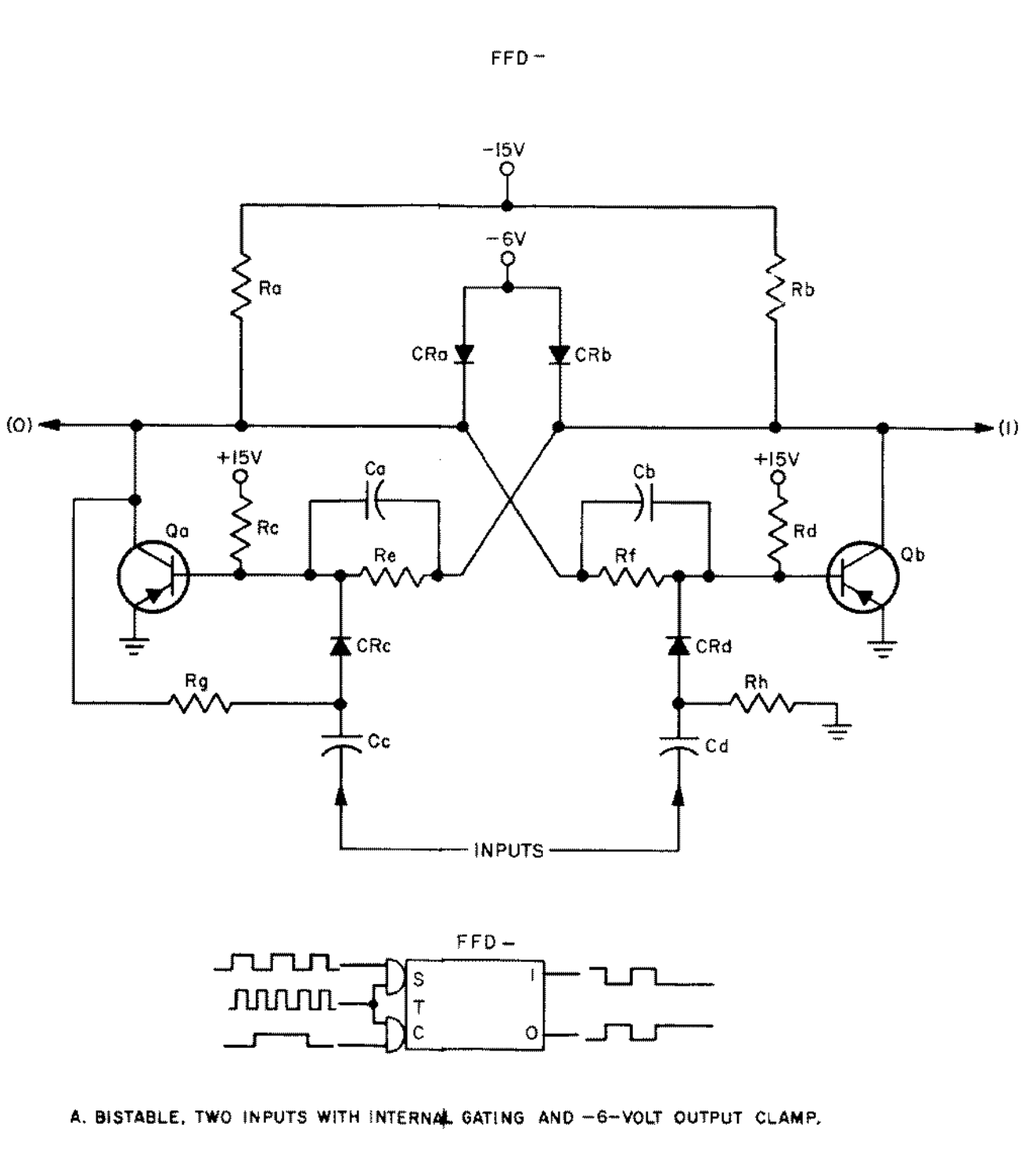
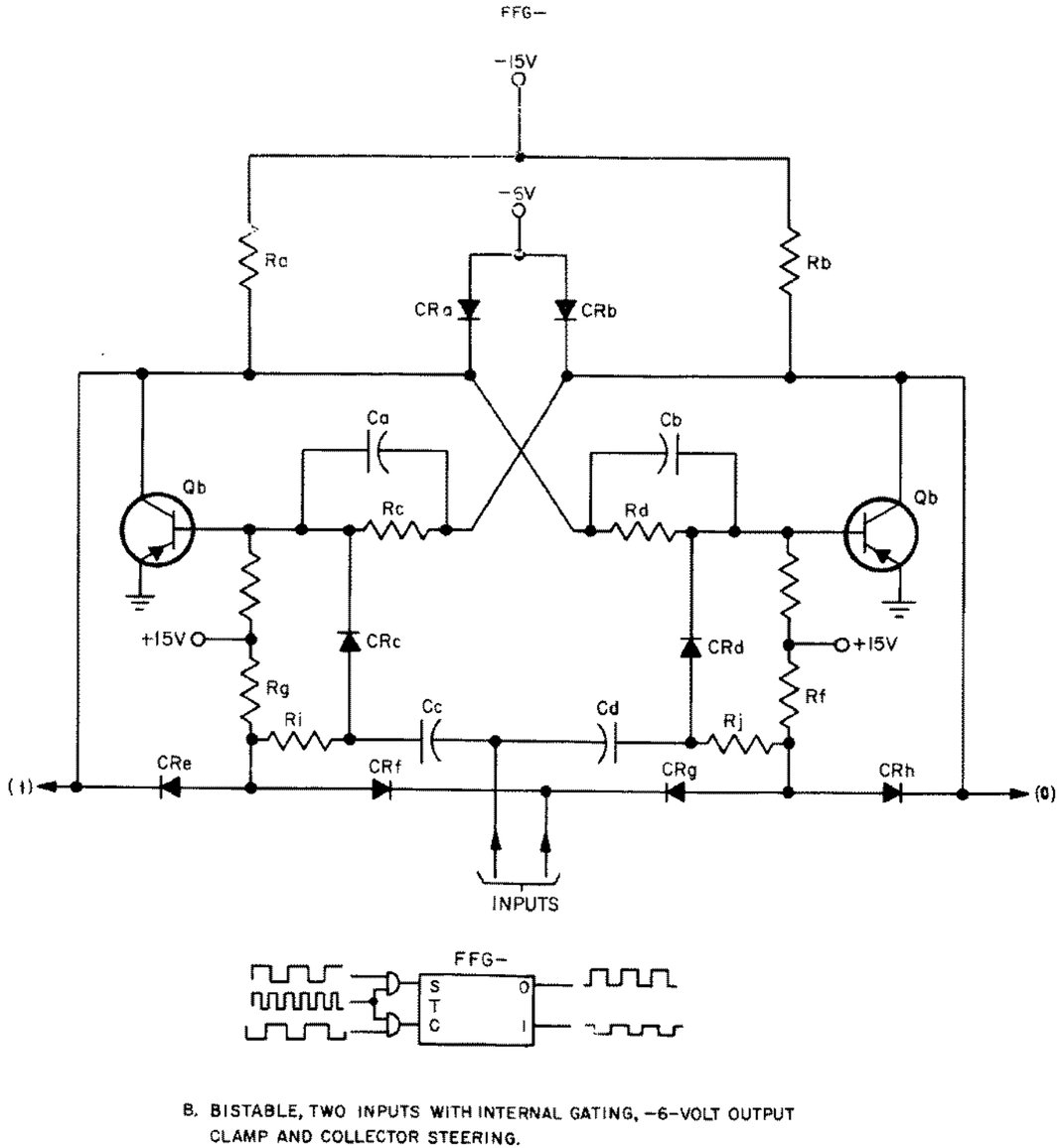


A. BISTABLE, TWO INPUTS WITH INTERNAL GATING AND –6–VOLT OUTPUT CLAMP.

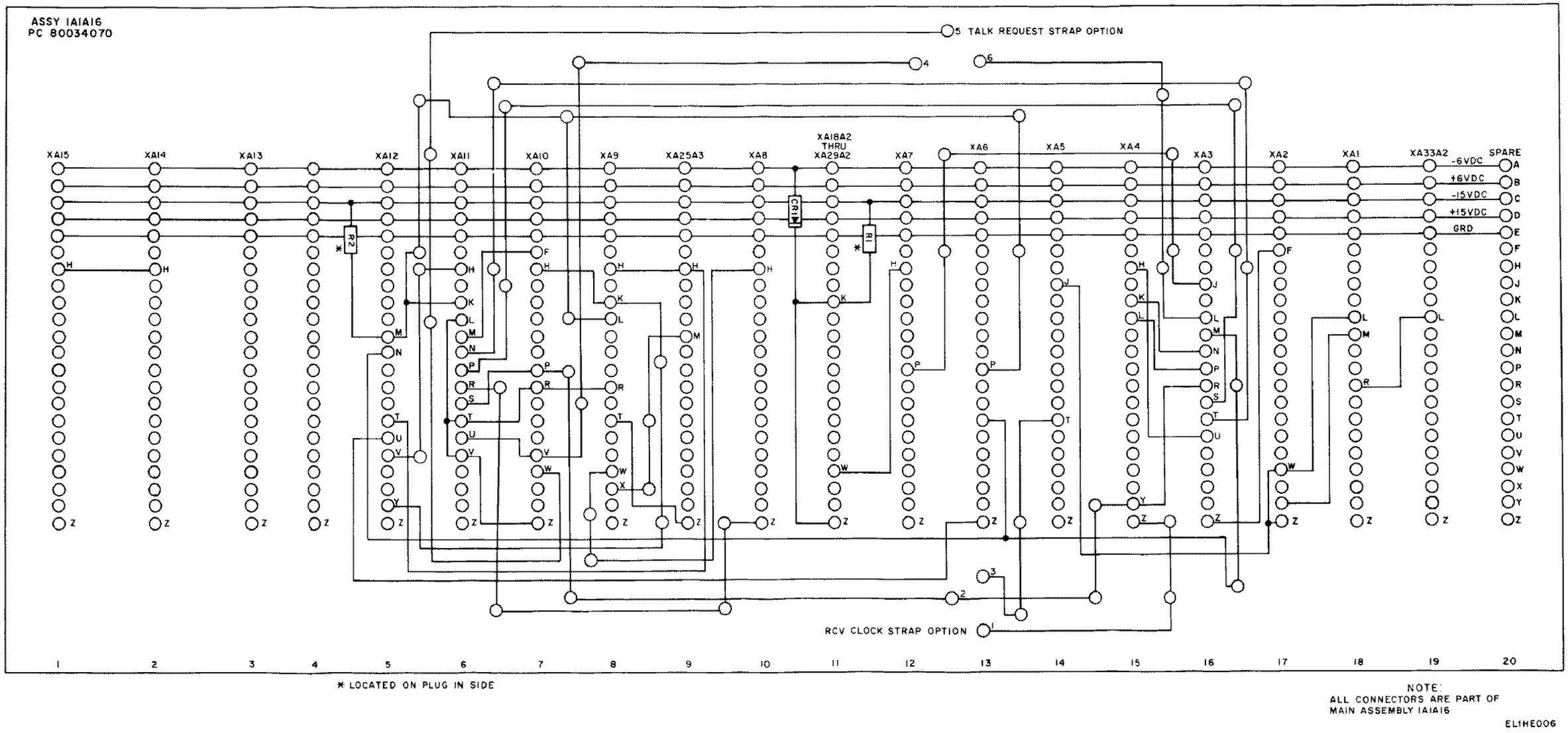


B. BISTABLE, TWO INPUTS WITH INTERNAL GATING, –6–VOLT OUTPUT CLAMP AND COLLECTOR STEERING.

EL1HE003

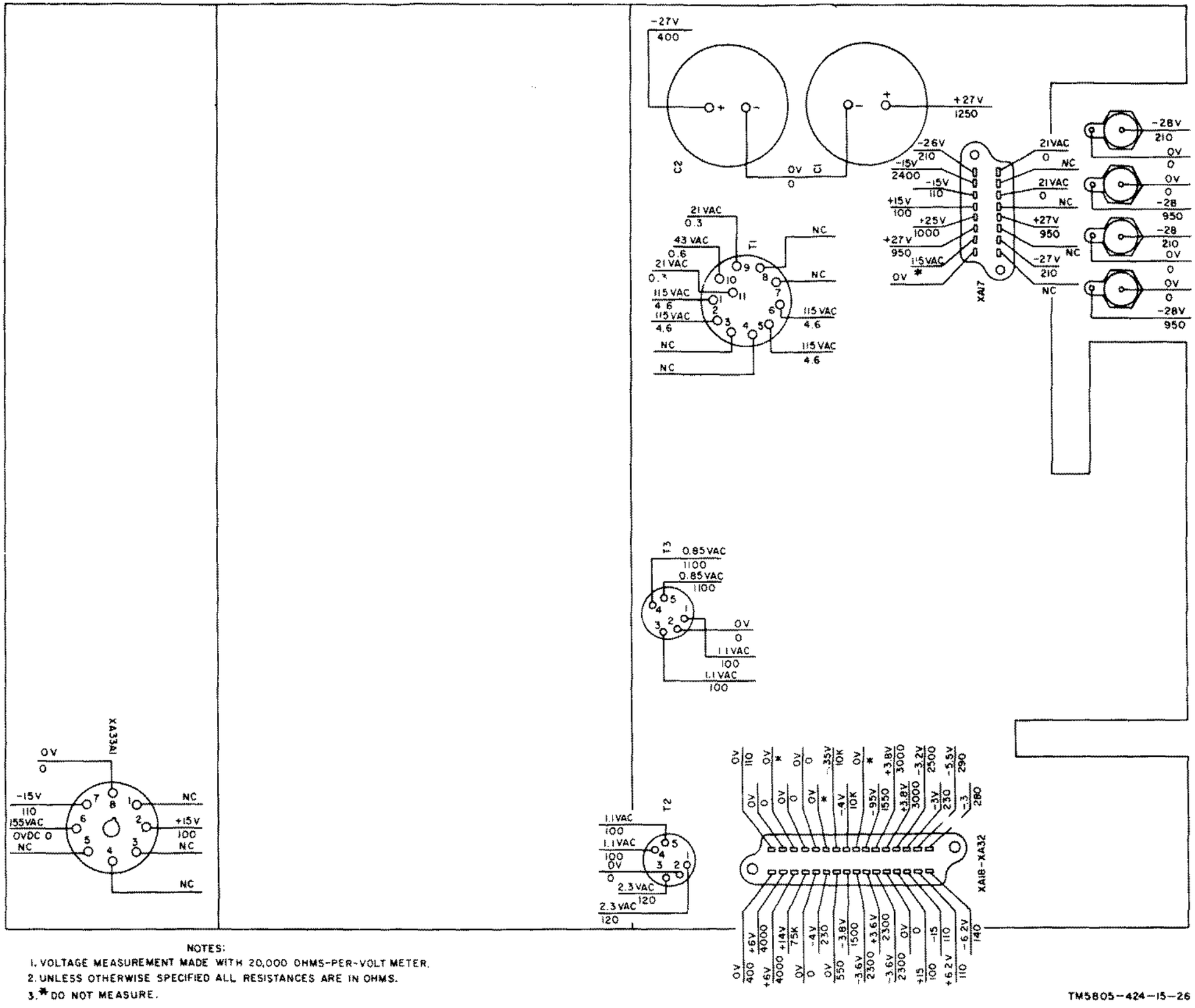
Change 5

■ **Figure 5-3. Two-input bistable stages, -6-volt clamped output, schematic diagram and logic symbol.**



Change 5

■ **Figure 6-17. printed-circuit card assembly A 16 (PC 80034070), harness card diagram.**



NOTES:
1. VOLTAGE MEASUREMENT MADE WITH 20,000 OHMS-PER-VOLT METER.
2. UNLESS OTHERWISE SPECIFIED ALL RESISTANCES ARE IN OHMS.
3. * DO NOT MEASURE.

TM5805-424-15-26

Figure 6-42, Main chassis voltage and resistance diagram.

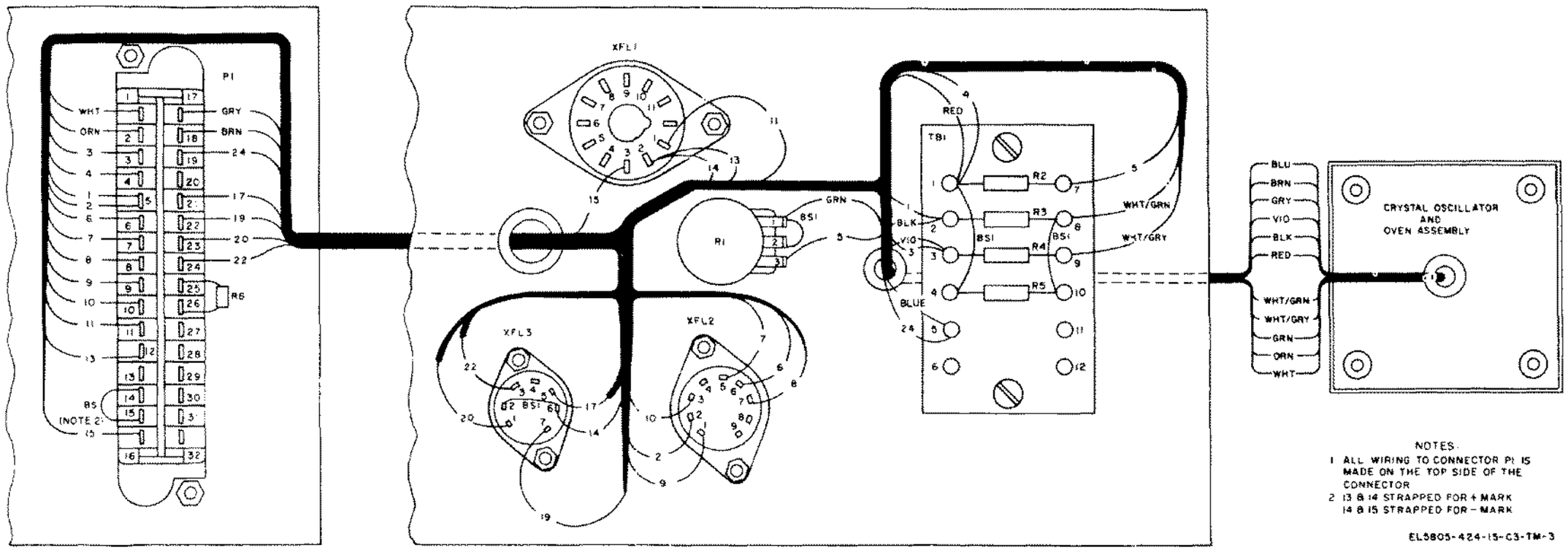


Figure 6-43. Plug-in module of Modem .;Subassembly MX-7372/ G. MX. 7374 / G, MX- 7376/ G, MX 7378 / G, MX-7380/ G, MX-7382/ G, MX-7384/ G, or MX-7386 / G, wiring diagram.

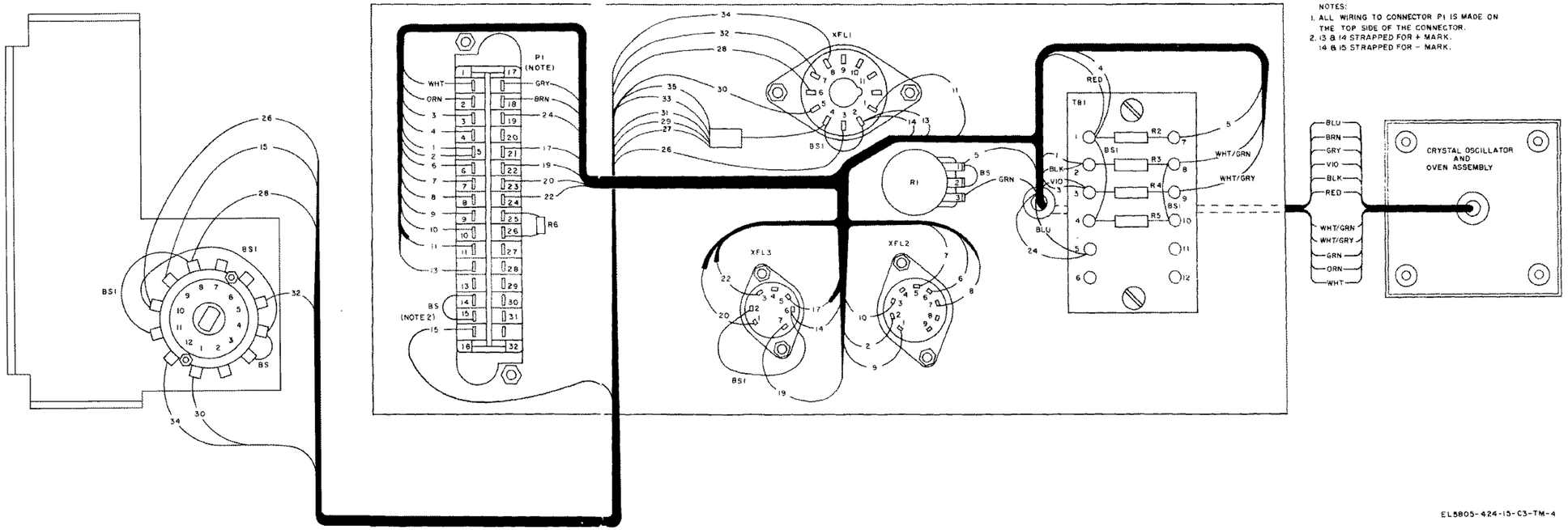


Figure 6-44. Plug-in module of Modem .;Subassembly MX-7373/ G. MX. 7375 / G, MX- 7377/ G, MX 7381 / G, MX-7383/ G, MX-7382/ G, MX-7385/ G, or MX-7385 / G, wiring diagram.

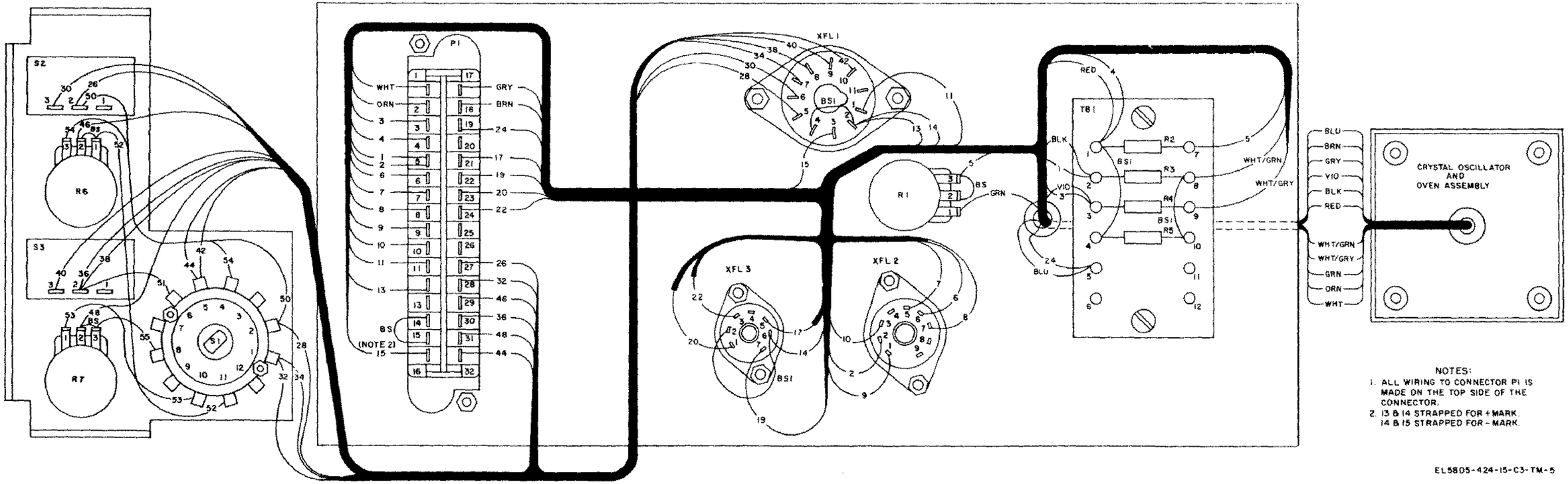


Figure 6-45. Plug-in module Subassembly MX-78379/G, wiring diagram.

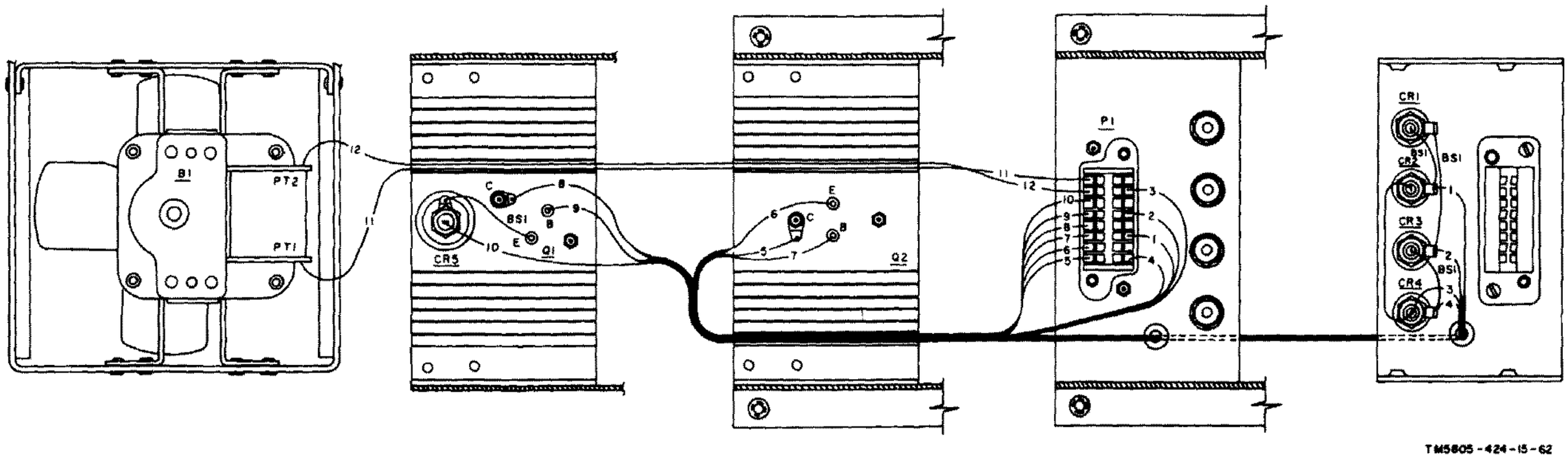


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Figure 6-46. Power supply submodule (assembly A1A17) wiring diagram

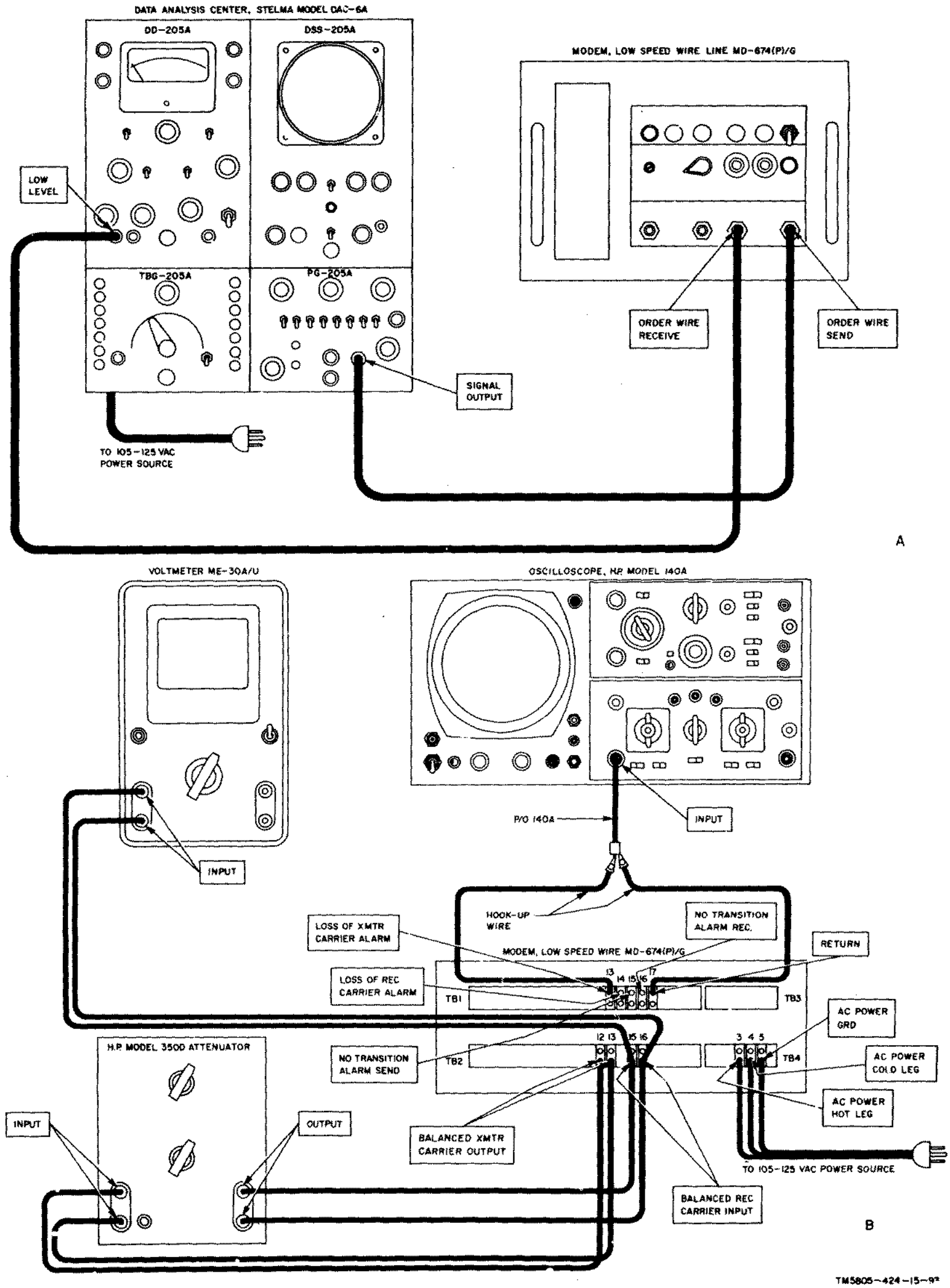
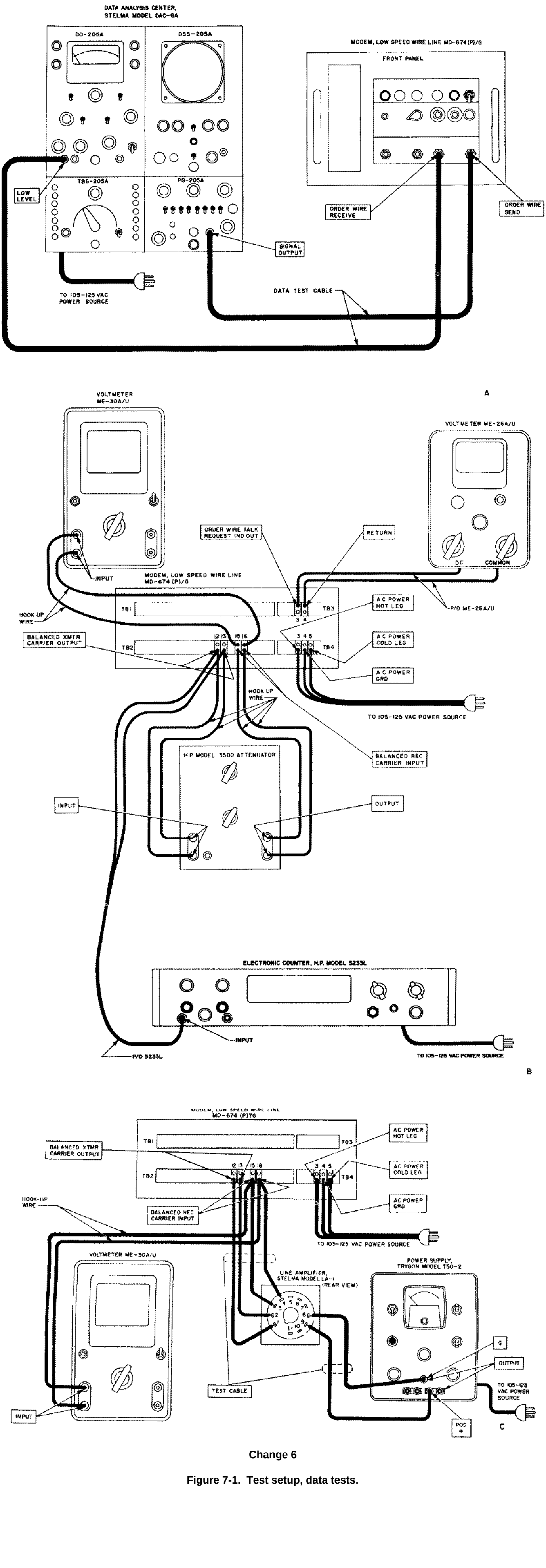
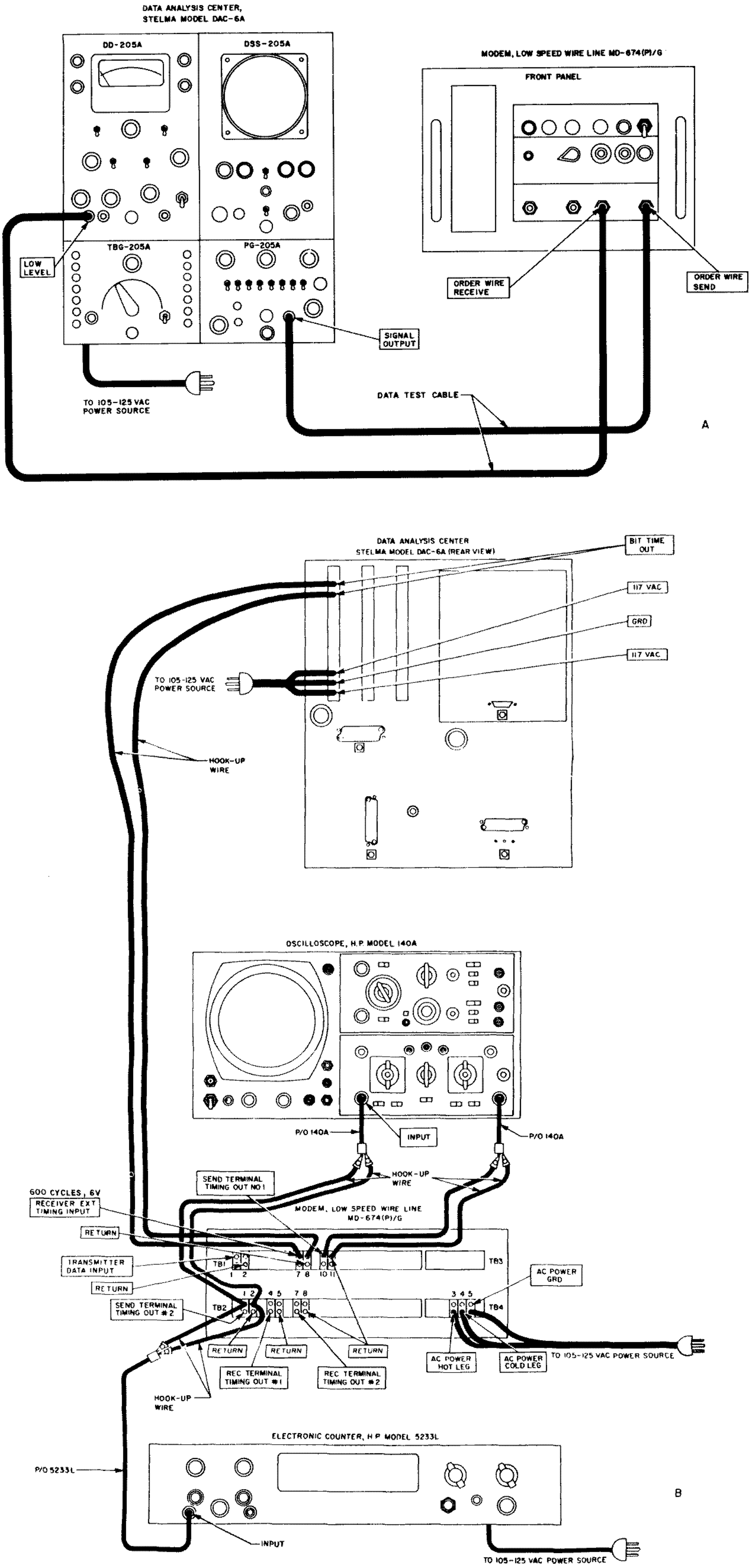


Figure 7-. Test setup, alarm test.



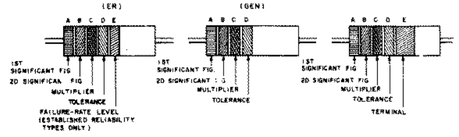
Change 6

Figure 7-1. Test setup, data tests.



Change 6

Figure 7-2. Test setup, timing tests.



COLOR CODE MARKING FOR COMPOSITION TYPE RESISTORS.

COLOR-CODE MARKING FOR FILM-TYPE RESISTORS

TABLE I
COLOR CODE FOR COMPOSITION TYPE AND FILM TYPE RESISTORS.

BAND A		BAND B		BAND C		BAND D		BAND E		
COLOR	FIRST SIGNIFICANT FIGURE	COLOR	SECOND SIGNIFICANT FIGURE	COLOR	MULTIPLIER	COLOR	RESISTANCE TOLERANCE (PERCENT)	COLOR	FAILURE RATE LEVEL	TERM.
BLACK	0	BLACK	0	BLACK	1			BROWN	M=1.0	
BROWN	1	BROWN	1	BROWN	10			RED	P=0.1	
RED	2	RED	2	RED	100			ORANGE	R=0.01	
ORANGE	3	ORANGE	3	ORANGE	1,000			YELLOW	S=0.001	
YELLOW	4	YELLOW	4	YELLOW	10,000	SILVER	±10 (COMP TYPE ONLY)	WHITE		SOLDERABLE
GREEN	5	GREEN	5	GREEN	100,000	GOLD	±5			
BLUE	6	BLUE	6	BLUE	1,000,000	RED	±2 (NOT APPLICABLE TO ESTABLISHED RELIABILITY)			
PURPLE (VIOLET)	7	PURPLE (VIOLET)	7							
GRAY	8	GRAY	8	SILVER	0.01					
WHITE	9	WHITE	9	GOLD	0.1					

BAND A — THE FIRST SIGNIFICANT FIGURE OF THE RESISTANCE VALUE (BANDS A THRU D SHALL BE OF EQUAL WIDTH.)

BAND B — THE SECOND SIGNIFICANT FIGURE OF THE RESISTANCE VALUE

BAND C — THE MULTIPLIER (THE MULTIPLIER IS THE FACTOR BY WHICH THE TWO SIGNIFICANT FIGURES ARE MULTIPLIED TO YIELD THE NOMINAL RESISTANCE VALUE.)

BAND D — THE RESISTANCE TOLERANCE.

BAND E — WHEN USED ON COMPOSITION RESISTORS, BAND E INDICATES ESTABLISHED RELIABILITY FAILURE-RATE LEVEL (PERCENT FAILURE PER 1,000 HOURS). ON FILM RESISTORS, THIS BAND SHALL BE APPROXIMATELY 1-1/2 TIMES THE WIDTH OF OTHER BANDS, AND INDICATES TYPE OF TERMINAL.

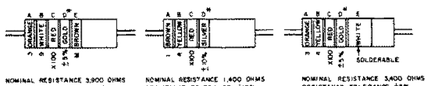
RESISTANCES IDENTIFIED BY NUMBERS AND LETTERS (THESE ARE NOT COLOR CODES.)

SOME RESISTORS ARE IDENTIFIED BY THREE OR FOUR DIGIT ALPHA NUMERIC DESIGNATORS. THE LETTER R IS USED IN PLACE OF A DECIMAL POINT WHEN FRACTIONAL VALUES OF AN OHM ARE EXPRESSED. FOR EXAMPLE:

2R7 = 2.7 OHMS 10R0 = 10.0 OHMS

FOR WIRE-WOUND-TYPE RESISTORS COLOR CODING IS NOT USED. IDENTIFICATION MARKING IS SPECIFIED IN EACH OF THE APPLICABLE SPECIFICATIONS.

EXAMPLES OF COLOR CODING



NOMINAL RESISTANCE 3,900 OHMS ±5% RESISTANCE TOLERANCE FAILURE RATE LEVEL M

NOMINAL RESISTANCE 1,400 OHMS RESISTANCE TOLERANCE ±10%

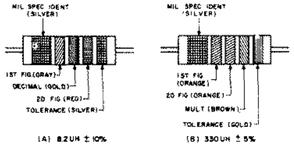
NOMINAL RESISTANCE 3,400 OHMS RESISTANCE TOLERANCE ±5% TERMINAL SOLDERABLE

COMPOSITION-TYPE RESISTORS

FILM-TYPE RESISTORS

* IF BAND D IS OMITTED, THE RESISTOR TOLERANCE IS ±20% AND THE RESISTOR IS NOT MIL-STD.

A COLOR CODE MARKING FOR MILITARY STANDARD RESISTORS.



COLOR CODING FOR TUBULAR ENCAPSULATED R.F. CHOKES. AT A, AN EXAMPLE OF OF THE CODING FOR AN 8.2UH CHOKE IS GIVEN. AT B, THE COLOR BANDS FOR A 330 UH INDUCTOR ARE ILLUSTRATED

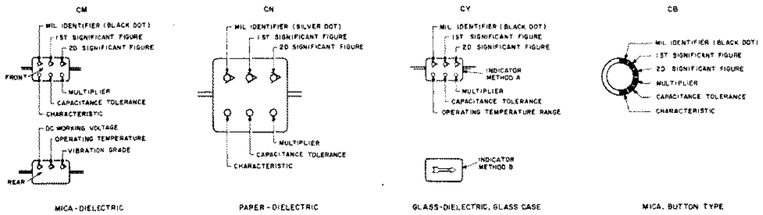
TABLE 2
COLOR CODING FOR TUBULAR ENCAPSULATED R.F. CHOKES

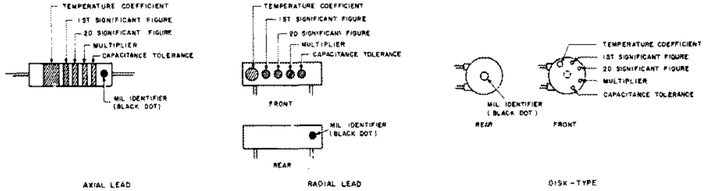
COLOR	SIGNIFICANT FIGURE	MULTIPLIER	INDUCTANCE TOLERANCE (PERCENT)
BLACK	0	1	
BROWN	1	10	1
RED	2	100	2
ORANGE	3	1,000	5
YELLOW	4		
GREEN	5		
BLUE	6		
VIOLET	7		
GRAY	8		
WHITE	9		
NONE			20
SILVER			10
GOLD	DECIMAL POINT		5

MULTIPLIER IS THE FACTOR BY WHICH THE TWO COLOR FIGURES ARE MULTIPLIED TO OBTAIN THE INDUCTANCE VALUE OF THE CHOKE COIL

B COLOR CODE MARKING FOR MILITARY STANDARD INDUCTORS.

CAPACITORS, FIXED, VARIOUS-DIELECTRICS, STYLES CM, CN, CY, AND CB





C. COLOR CODE MARKING FOR MILITARY STANDARD CAPACITORS.

TABLE 3 — FOR USE WITH STYLES CM, CN, CY AND CB.

COLOR	MIL ID	1ST SIG FIG	2D SIG FIG	MULTIPLIER	CAPACITANCE TOLERANCE CM	CN	CY	CB	CHARACTERISTIC CM	CN	CB	DC WORKING VOLTAGE CM	CY	OPERATING TEMP RANGE CM, CN	VIBRATION GRADE CM
BLACK	CM, CY, CN	0	0	1			±20%	±20%	A					-55° TO +70°C	10-55 HZ
BROWN		1	1	10					B	E	B				
RED		2	2	100	±2%		±2%	±2%	C					-55° TO +85°C	
ORANGE		3	3	1,000	±30%				D		D	500			
YELLOW		4	4	10,000					E					-55° TO +125°C	10-2,000HZ
GREEN		5	5		±5%				F			500			
BLUE		6	6											-55° TO +150°C	
PURPLE (VIOLET)		7	7												
GRAY		8	8												
WHITE		9	9												
GOLD				0.1			±5%	±5%							
SILVER	CN			0.01	±10%	±10%	±10%	±10%							

TABLE 4 — TEMPERATURE COMPENSATING, STYLE CC.

COLOR	TEMPERATURE COEFFICIENT	1ST SIG FIG	2D SIG FIG	MULTIPLIER	CAPACITANCE TOLERANCE: CAPACITANCES OVER 10 UUF	CAPACITANCES 10 UUF OR LESS	MIL ID
BLACK	0	0	0	1		±2.0 UUF	CC
BROWN	-30	1	1	10	±1%		
RED	-60	2	2	100	±2%	±0.25 UUF	
ORANGE	-150	3	3	1,000			
YELLOW	-220	4	4				
GREEN	-330	5	5		±5%	±0.5 UUF	
BLUE	-470	6	6				
PURPLE (VIOLET)	-750	7	7				
GRAY		8	8	0.01*			
WHITE		9	9	0.1*	±10%		
GOLD	+100			0.1		±1.0 UUF	
SILVER				0.01			

1. THE MULTIPLIER IS THE NUMBER BY WHICH THE TWO SIGNIFICANT (SIG) FIGURES ARE MULTIPLIED TO OBTAIN THE CAPACITANCE IN UUF.
2. LETTERS INDICATE THE CHARACTERISTICS DESIGNATED IN APPLICABLE SPECIFICATIONS. MIL-C-5, MIL-C-250, MIL-C-11272B, AND MIL-C-10950C RESPECTIVELY.
3. LETTERS INDICATE THE TEMPERATURE RANGE AND VOLTAGE-TEMPERATURE LIMITS DESIGNATED IN MIL-C-11015D.
4. TEMPERATURE COEFFICIENT IN PARTS PER MILLION PER DEGREE CENTIGRADE.
* OPTIONAL CODING WHERE METALLIC PIGMENTS ARE UNDESIRABLE.

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Figure 8-3. Color code markings for MIL-STD resistors, capacitors, and inductors.

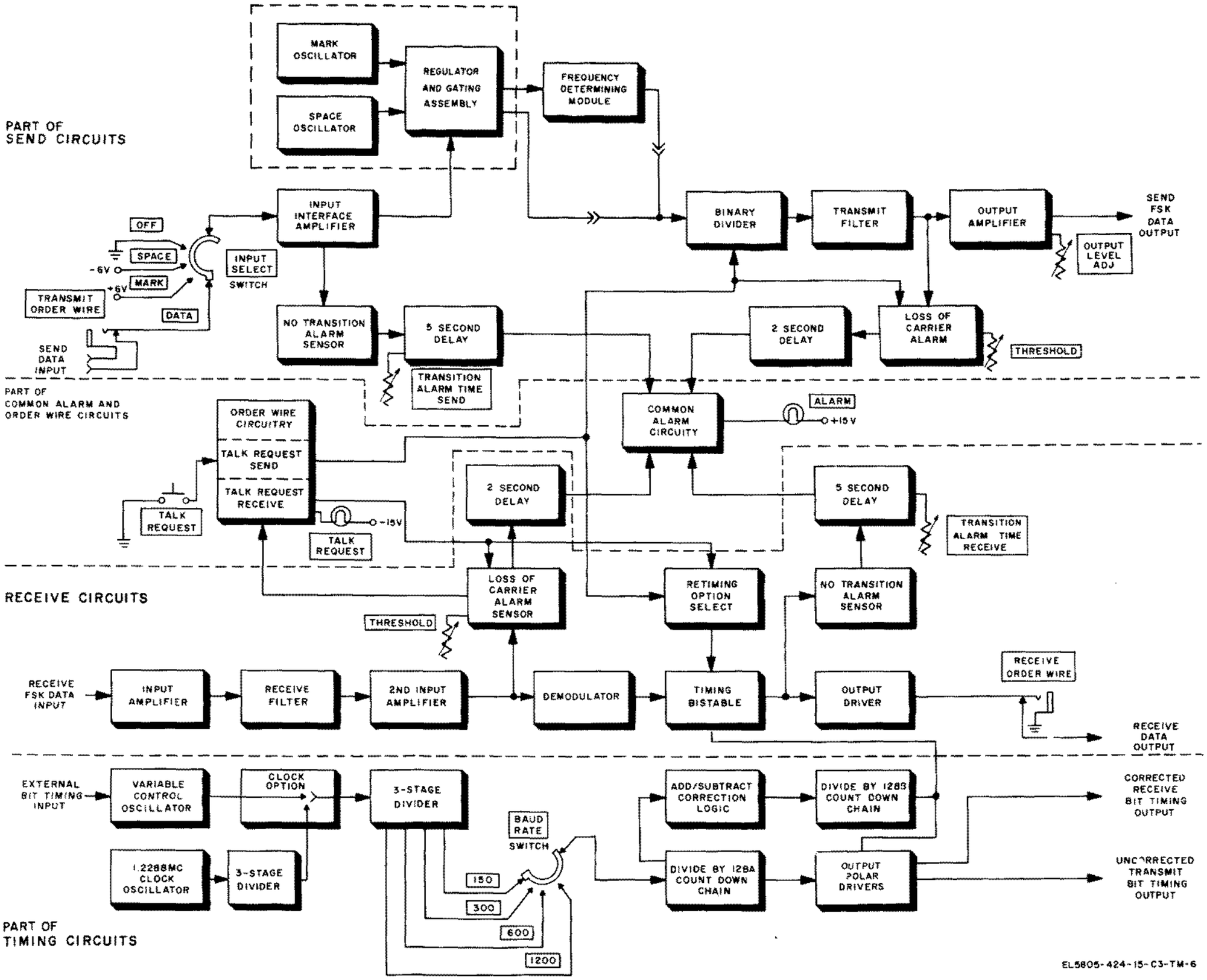


Figure 8-4. Modem, low speed wire line MD-674 (P)/G, block diagram.

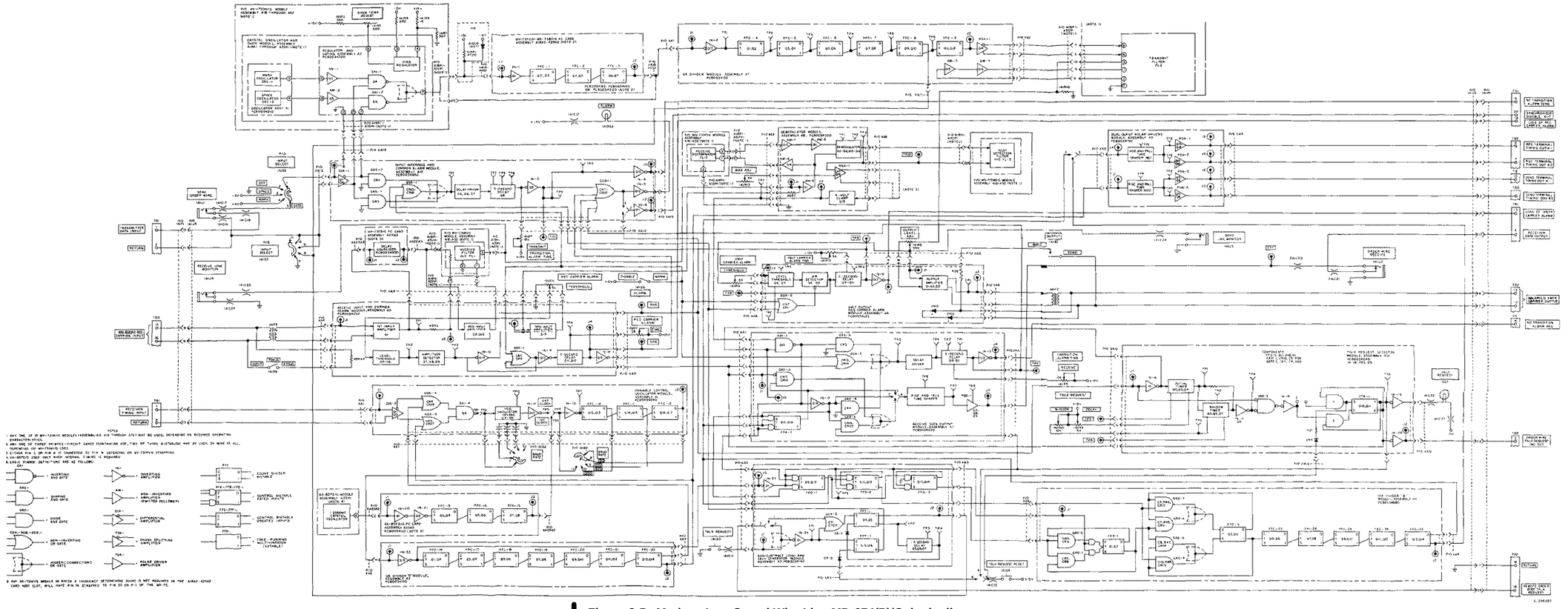


Figure 8-5. Modem, Low Speed Wire Line MD-674(P)/G, logic diagram.

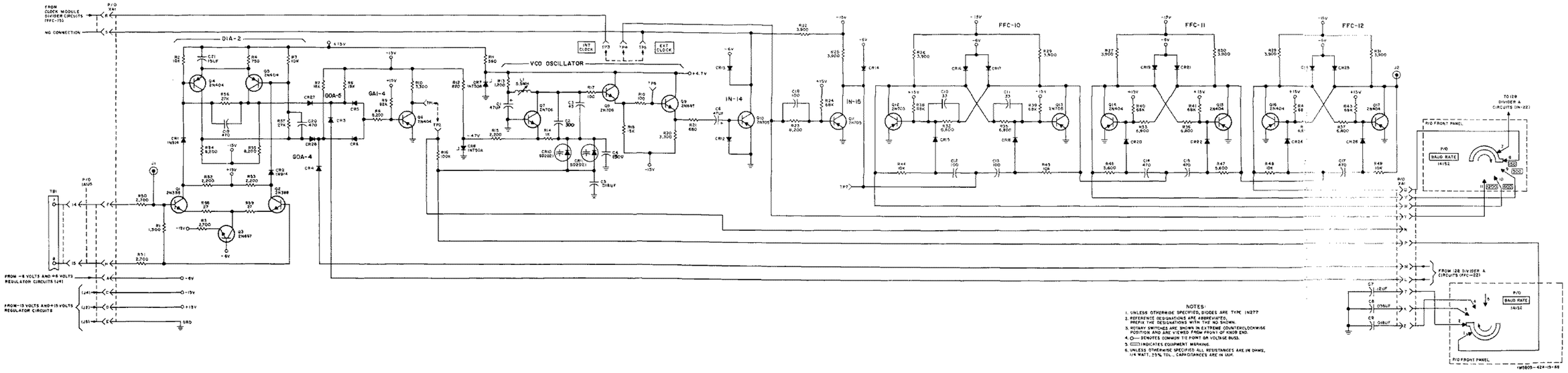


Figure 8-6. Variable-control oscillator circuits assembly A1 (PC 80034090) schematic diagram.

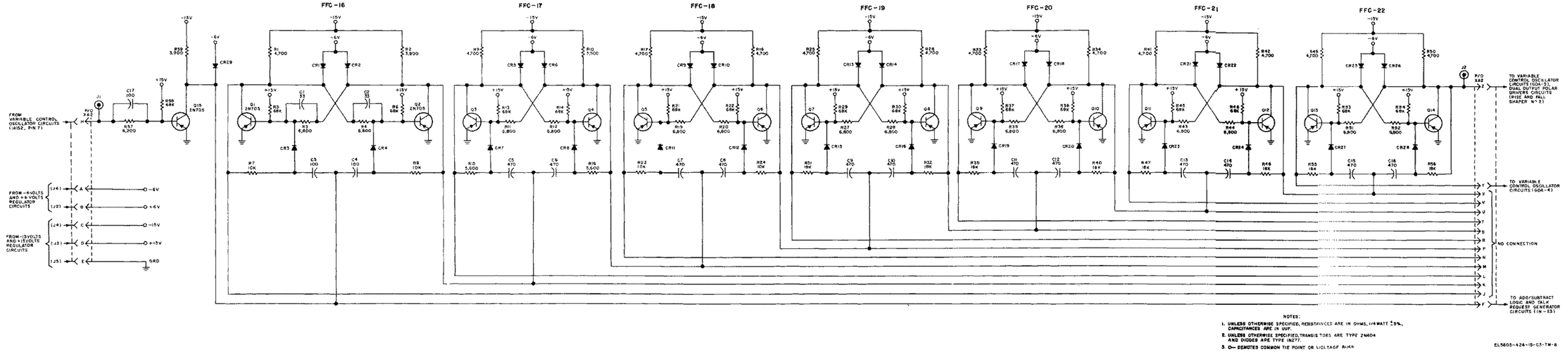


Figure 8-7. 128 divider-A circuits assembly A2 (PC80034100), schematic diagram.

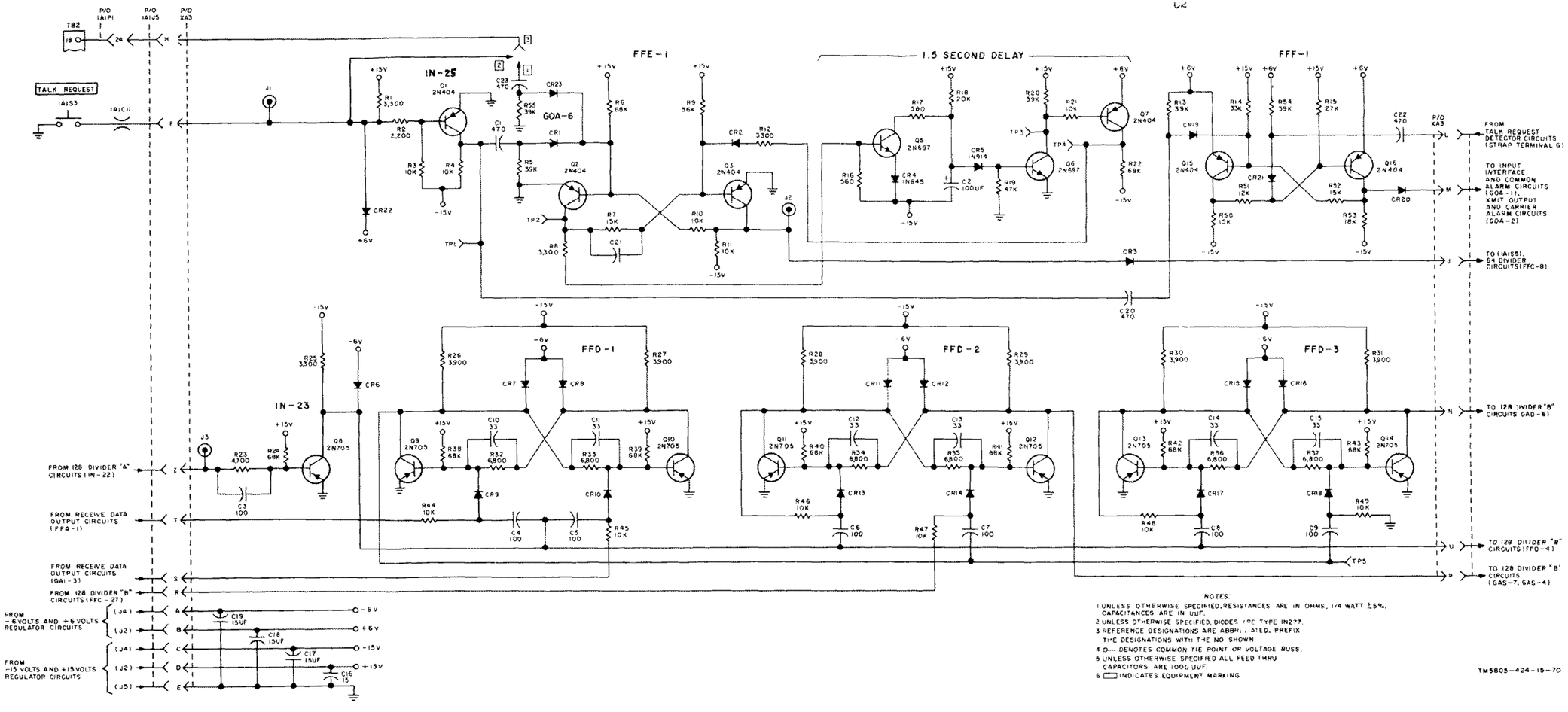


Figure 8-8. Add-subtract logic and talk request generator circuits assembly A3 (PC 80034140), schematic diagram.

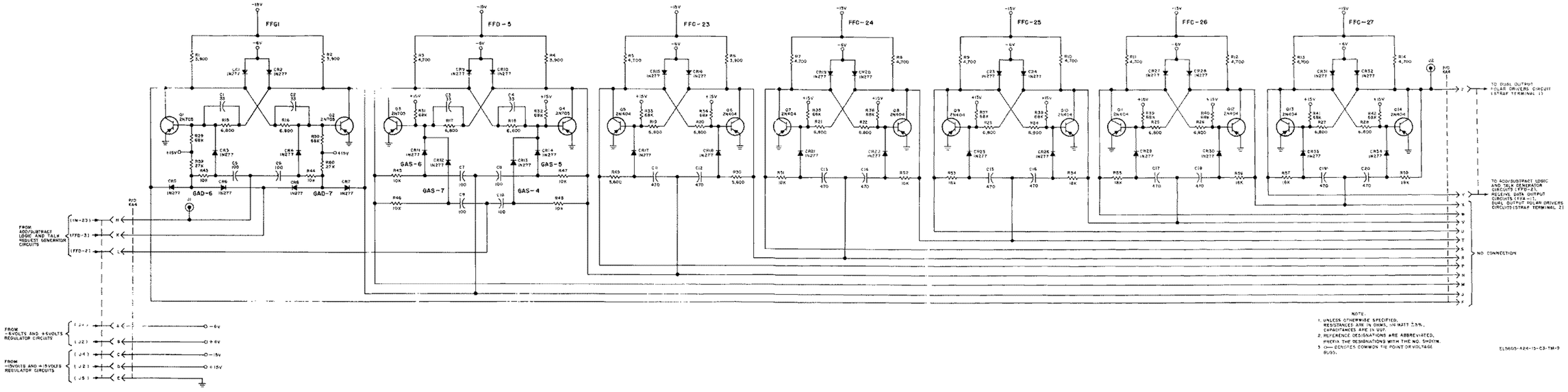


Figure 8-9. 128 divider-B circuits assembly A4 (PC80034080), schematic diagram.

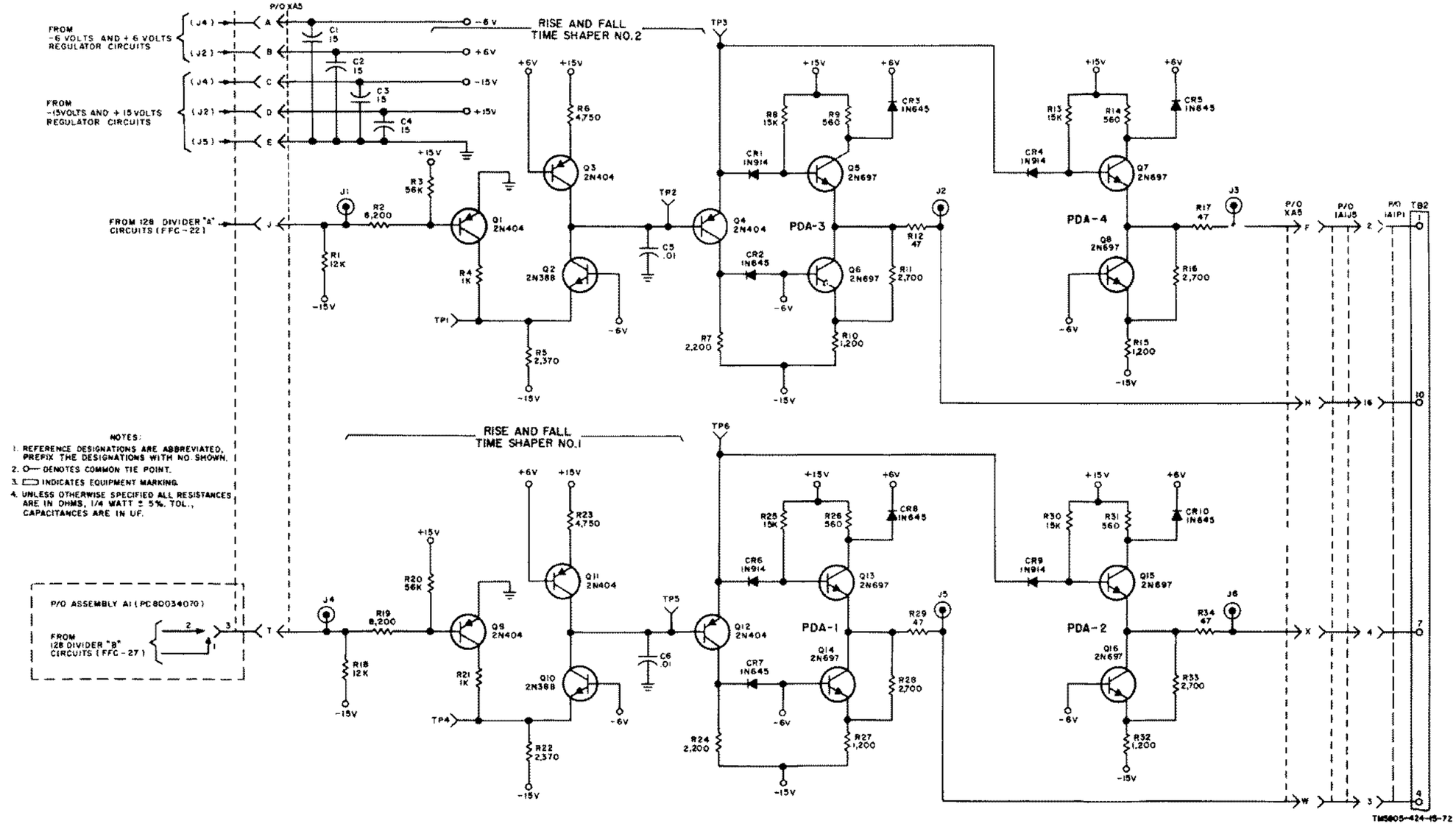


Figure 8-10. Dual output polar driver circuits assembly A5 (PC 80034150), schematic diagram.

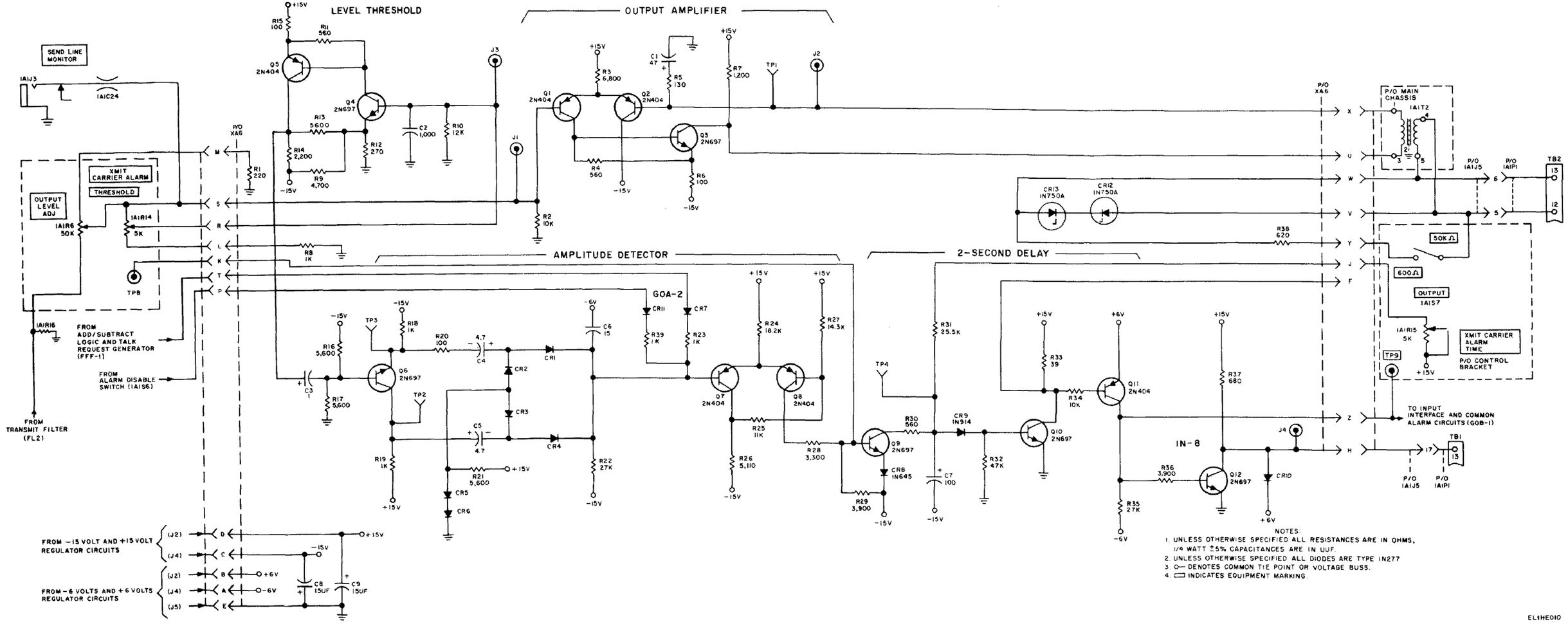


Figure 8-11. Transmit output aid carrier alarm circuits assembly A 6 (PC 80034120), schematic diagram.

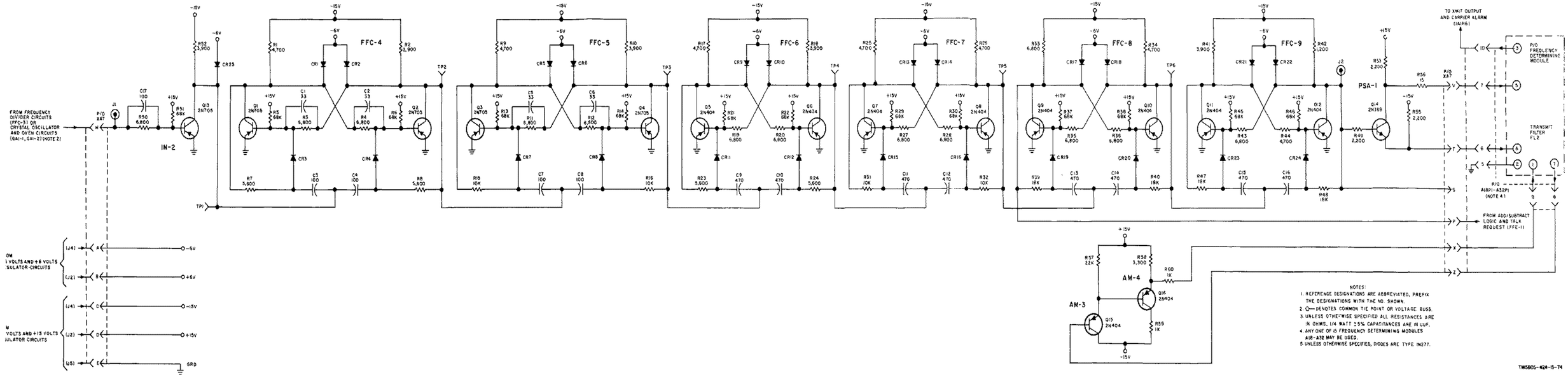


Figure 8-12. 64 divider circuits assembly A7 (PC 80034130. schematic diagram.

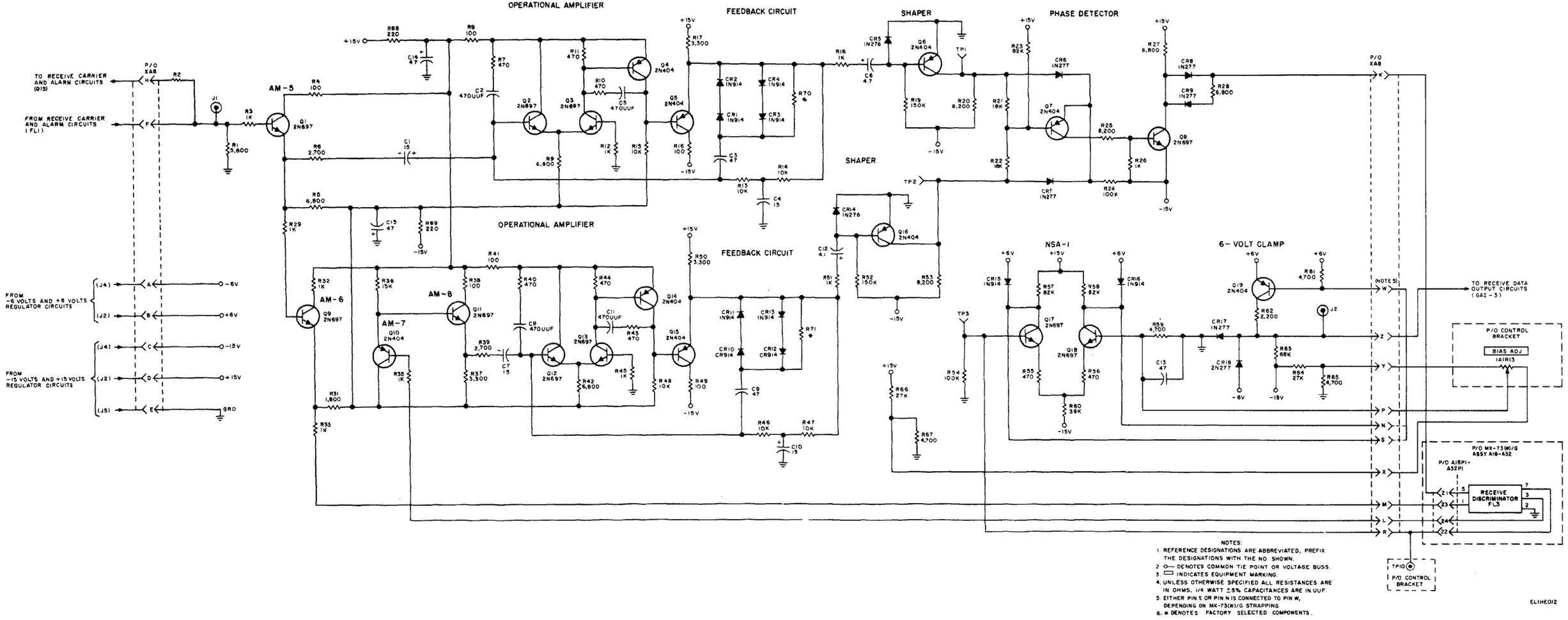


Figure 8-13. Demodulator circuits assembly A8 (PC 80034020), schematic diagram.

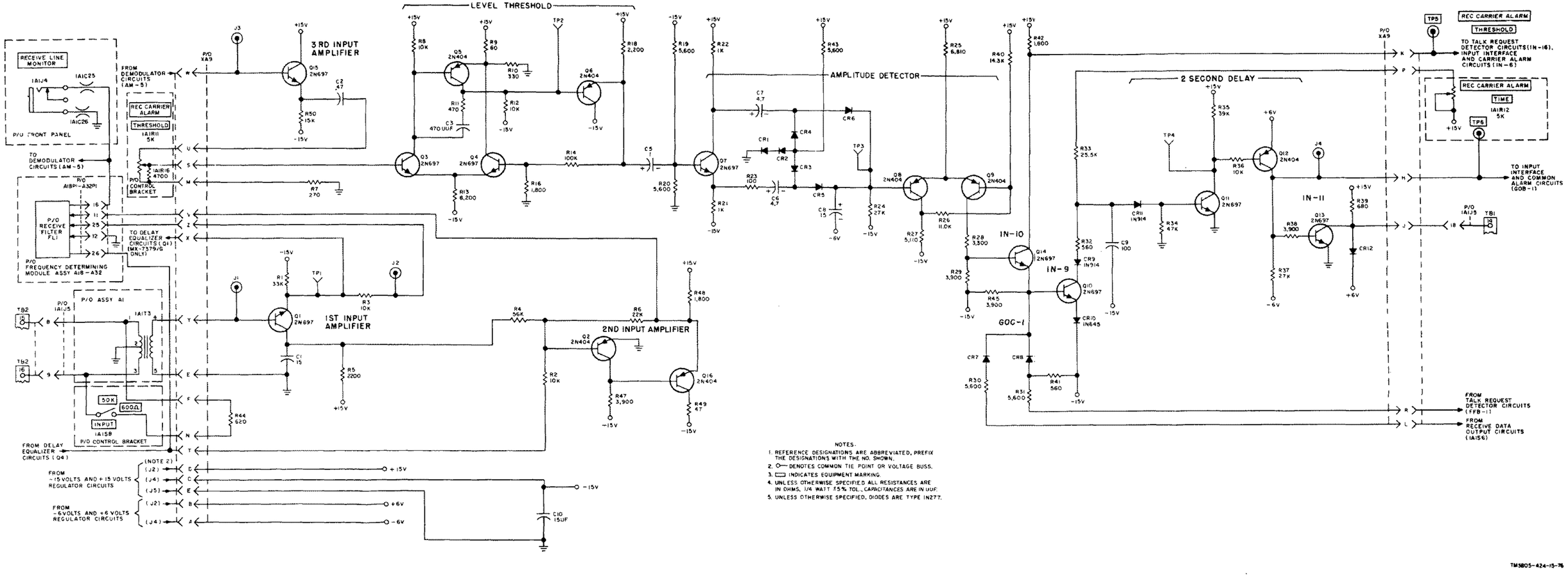


Figure 8-14. Receive input and carrier alarm circuits assembly A9 (PC 80034050), schematic diagram.

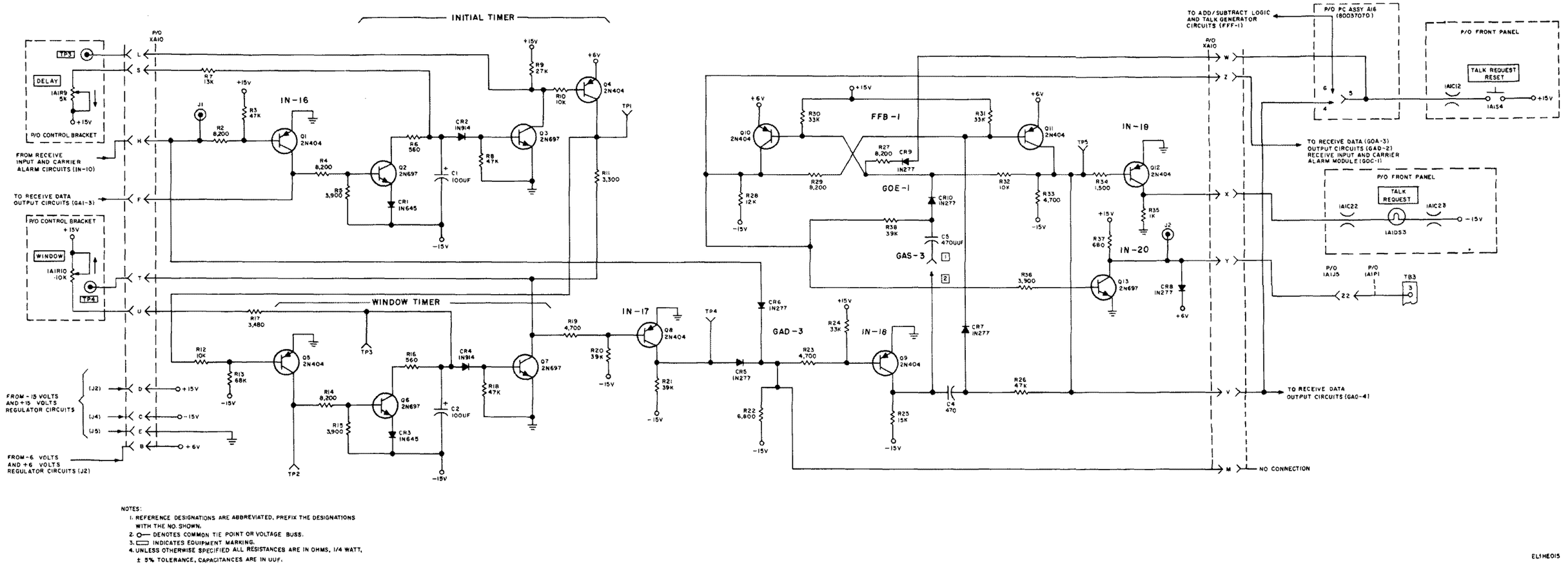


Figure 8-15. Talk-request detector circuits assembly A10 (PC 80034040), schematic diagram.

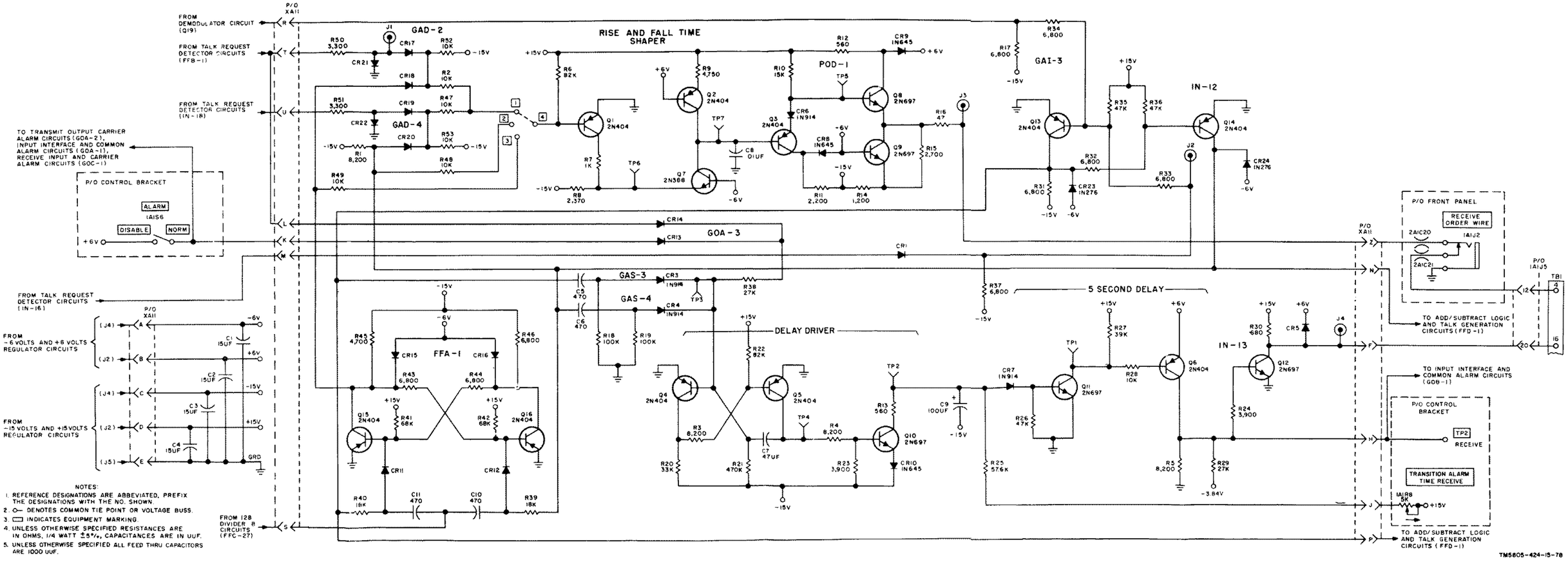


Figure 8-16. Receive data output circuits assembly A11 (PC 80034030), schematic diagram.

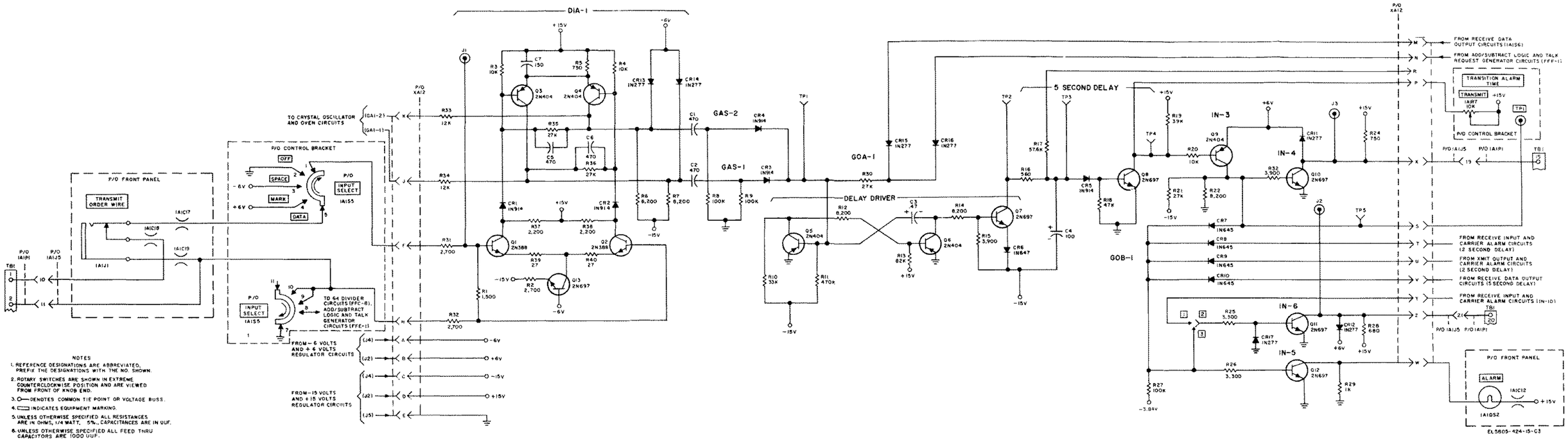


Figure 8-17. Input interface and common alarm circuits assembly A12 (PC80034060), schematic diagram.

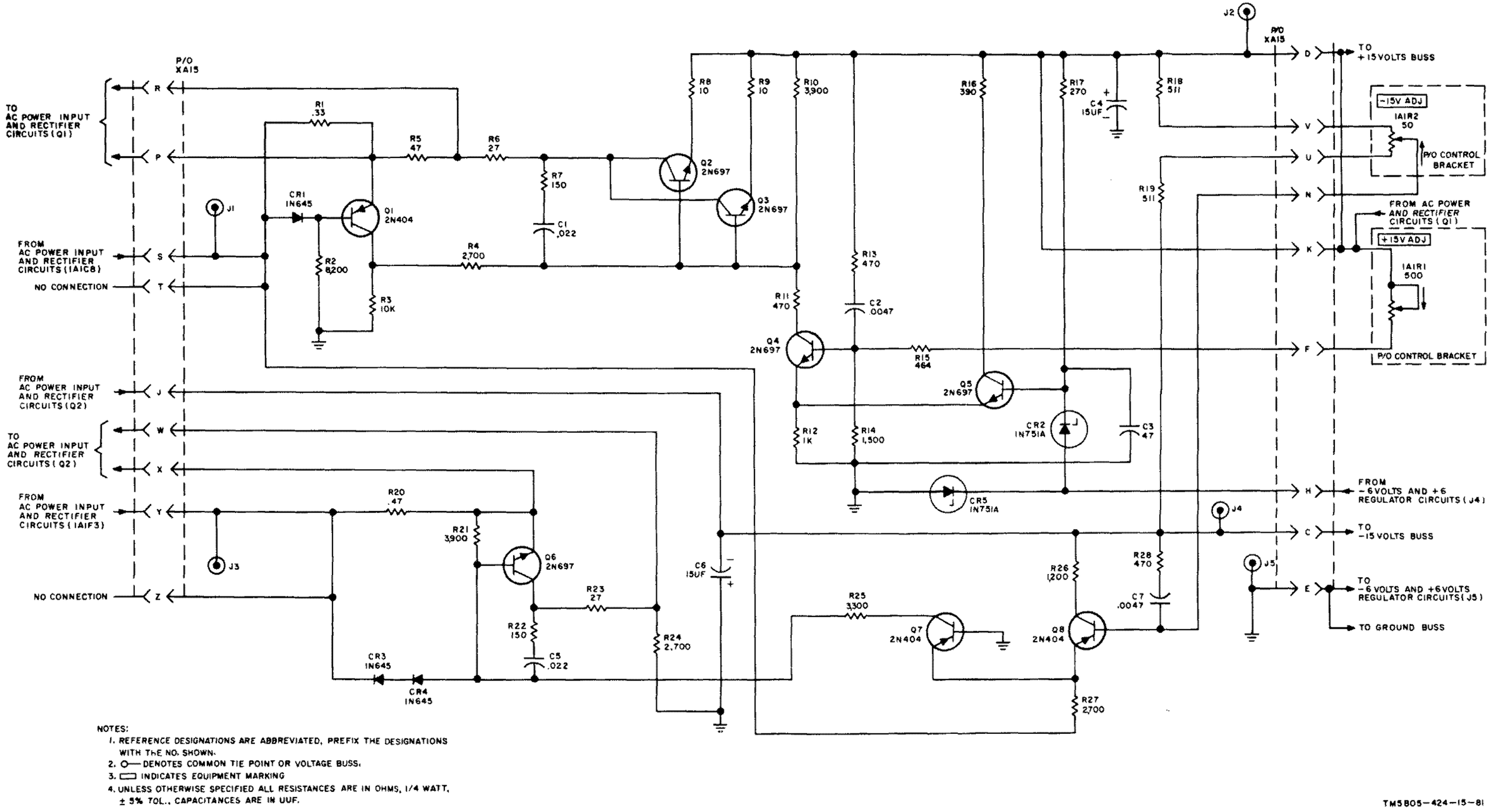
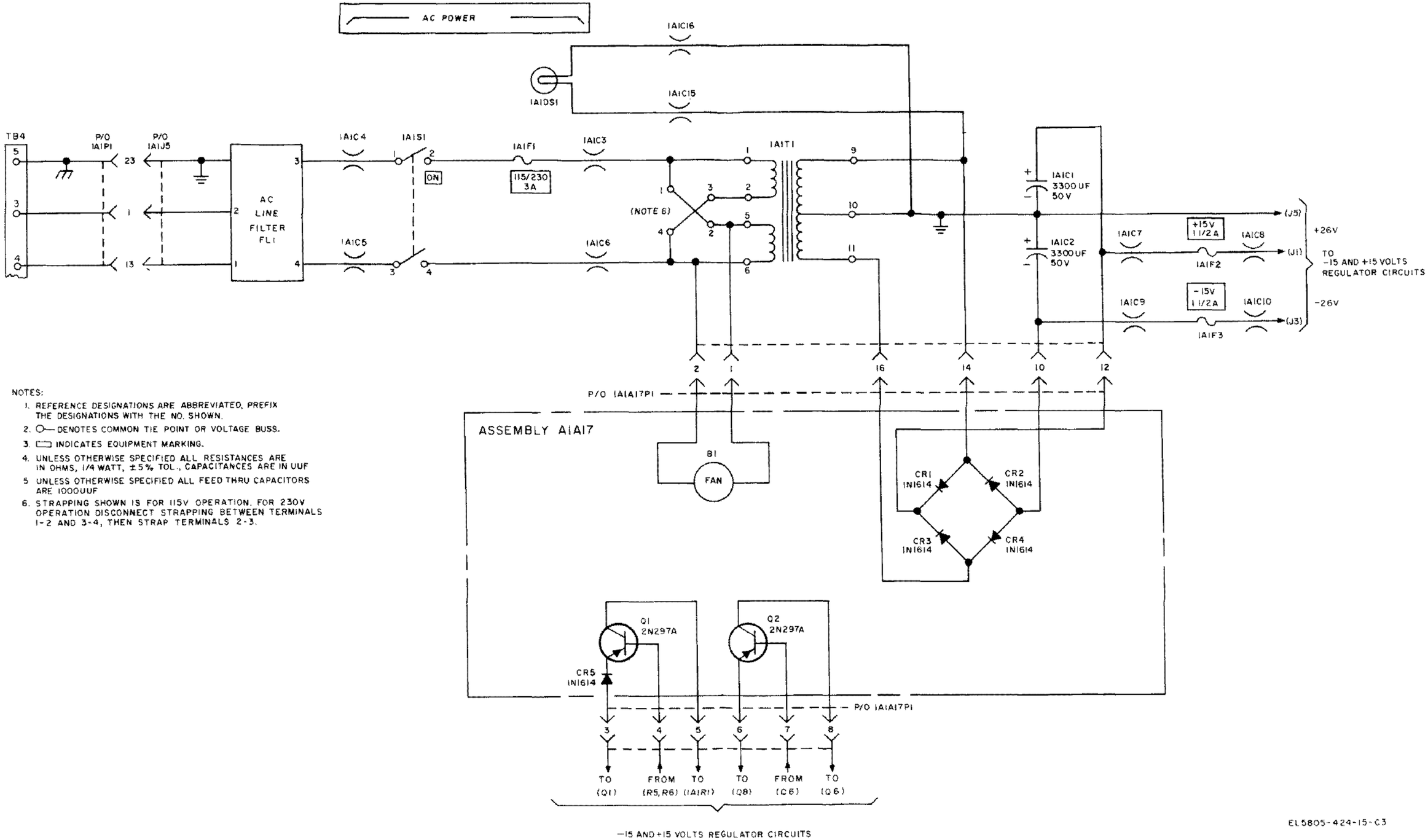


Figure 8-19. ±15-volt power supply regulator circuits assembly A15 (PC 80034160), schematic diagram.



NOTES:

1. REFERENCE DESIGNATIONS ARE ABBREVIATED, PREFIX THE DESIGNATIONS WITH THE NO. SHOWN.
2. ○— DENOTES COMMON TIE POINT OR VOLTAGE BUSS.
3. ▭ INDICATES EQUIPMENT MARKING.
4. UNLESS OTHERWISE SPECIFIED ALL RESISTANCES ARE IN OHMS, 1/4 WATT, ±5% TOL., CAPACITANCES ARE IN UUF
5. UNLESS OTHERWISE SPECIFIED ALL FEED THRU CAPACITORS ARE 1000UUF
6. STRAPPING SHOWN IS FOR 115V OPERATION. FOR 230V OPERATION DISCONNECT STRAPPING BETWEEN TERMINALS 1-2 AND 3-4, THEN STRAP TERMINALS 2-3.

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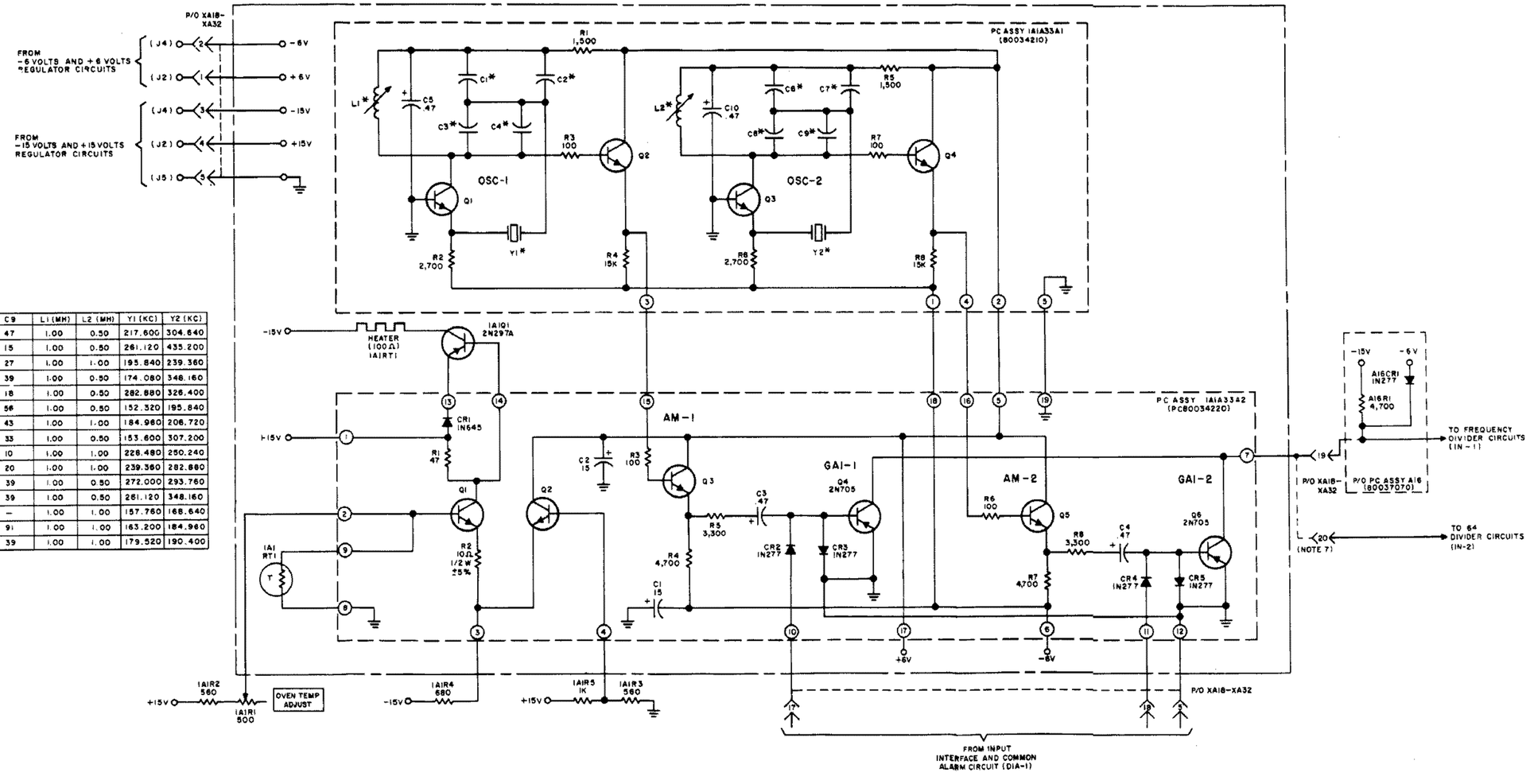
Figure 8-20. Ac power and rectifier circuit, modem chassis, and power supply submodule, schematic diagram.



NOTES:
1. REFERENCE DESIGNATIONS ARE ABBREVIATED, PREFIX THE DESIGNATIONS WITH THE NO. SHOWN.
2. ⏀ DENOTES COMMON TIE POINT OR VOLTAGE BUSS.
3. ▭ INDICATES EQUIPMENT MARKING.
4. UNLESS OTHERWISE SPECIFIED ALL RESISTANCES ARE IN OHMS, 1/4 WATT ±5%, CAPACITANCES ARE IN UUF.
5. UNLESS OTHERWISE SPECIFIED ALL TRANSISTORS ARE TYPE 2N706.
6. * DENOTES FACTORY SELECTED COMPONENTS.

MX (*)	C1	C2	C3	C4	C6	C7	C8	C9	L1 (MH)	L2 (MH)	Y1 (KC)	Y2 (KC)
MX-7372/G	2,400	180	620	27	2,400	270	620	47	1.00	0.50	217.600	304.640
MX-7373/G	1,800	10	430	22	1,200	56	300	15	1.00	0.50	261.120	435.200
MX-7374/G	3,000	220	750	56	2,000	150	510	27	1.00	1.00	195.840	239.360
MX-7375/G	3,900	180	1,000	22	2,000	24	470	39	1.00	0.50	174.080	348.160
MX-7376/G	1,500	20	360	20	2,200	100	560	18	1.00	0.50	282.880	326.400
MX-7377/G	4,700	620	1,300	39	3,000	220	750	56	1.00	0.50	152.320	195.840
MX-7378/G	3,600	36	820	91	2,700	200	680	43	1.00	1.00	184.980	206.720
MX-7379/G	4,700	560	1,300	22	2,400	200	620	33	1.00	0.50	153.600	307.200
MX-7380/G	2,200	130	560	22	1,800	120	470	10	1.00	1.00	228.480	250.240
MX-7381/G	2,000	150	510	27	1,500	20	360	20	1.00	1.00	239.360	282.880
MX-7382/G	1,600	39	390	20	2,700	180	680	39	1.00	0.50	272.000	293.760
MX-7383/G	1,800	10	430	22	2,000	24	470	39	1.00	0.50	261.120	348.160
MX-7384/G	4,700	300	1,200	51	4,300	100	1,100	—	1.00	1.00	157.760	168.640
MX-7385/G	4,300	390	1,100	68	3,600	36	820	91	1.00	1.00	163.200	184.960
MX-7386/G	3,600	240	910	51	3,300	150	820	39	1.00	1.00	179.520	190.400

7. AN MX-73(M)/G MODULE IN WHICH A FREQUENCY DETERMINING BOARD IS NOT REQUIRED IN THE A18A2-A29A2 SLOT IN THE CARD NEST WILL HAVE PIN 19 STRAPPED TO PIN 20 ON PI OF THE MX-73(M)/G.

Figure 8-21. Crystal oscillator and regulator circuit assemblies A1A18A1-A32A1A1 and A18A1A2-A32A1A2 (PC 80034210, PC80034220), schematic diagram.

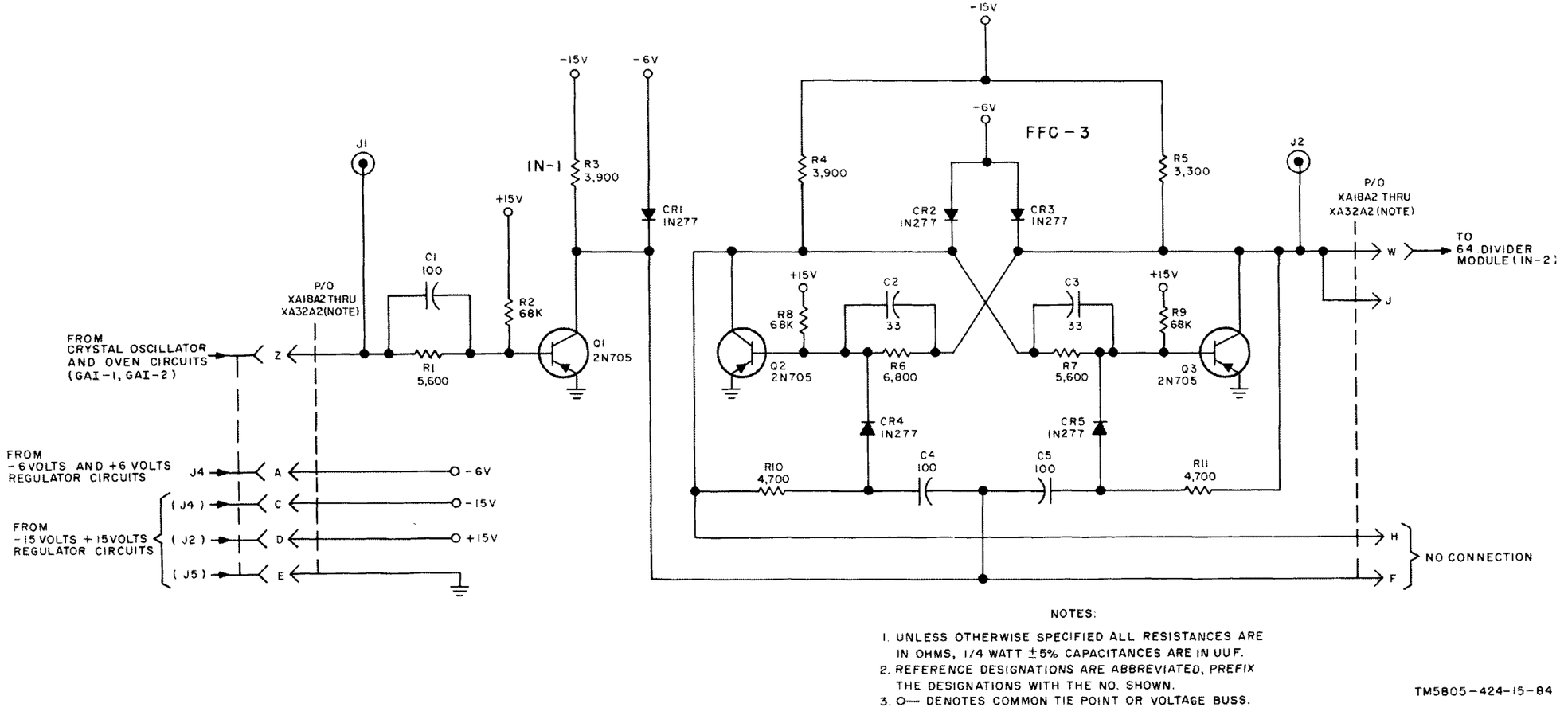


Figure 8-22. One-stage frequency divider circuit assemblies A23A2-A292 (PC 80034180), schematic diagram.

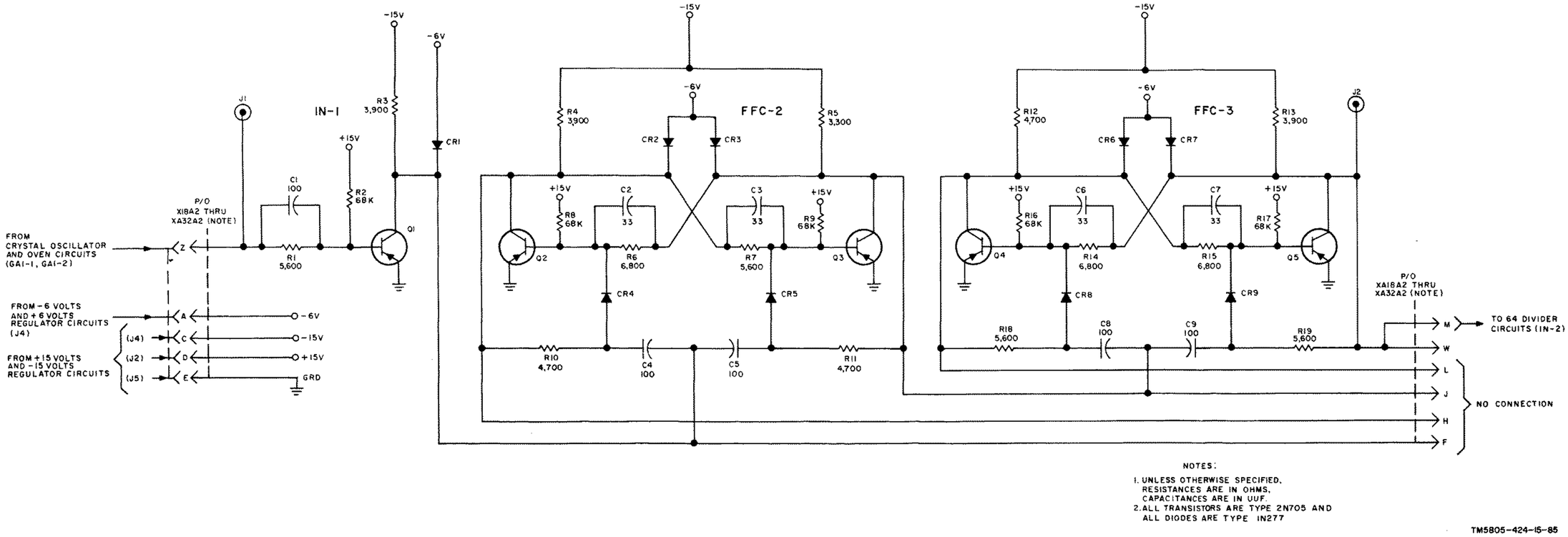


Figure 8-23. Two-stage frequency divider circuit assemblies A20A2, A21A2, and A22A2 (PC 80034190) schematic diagram.

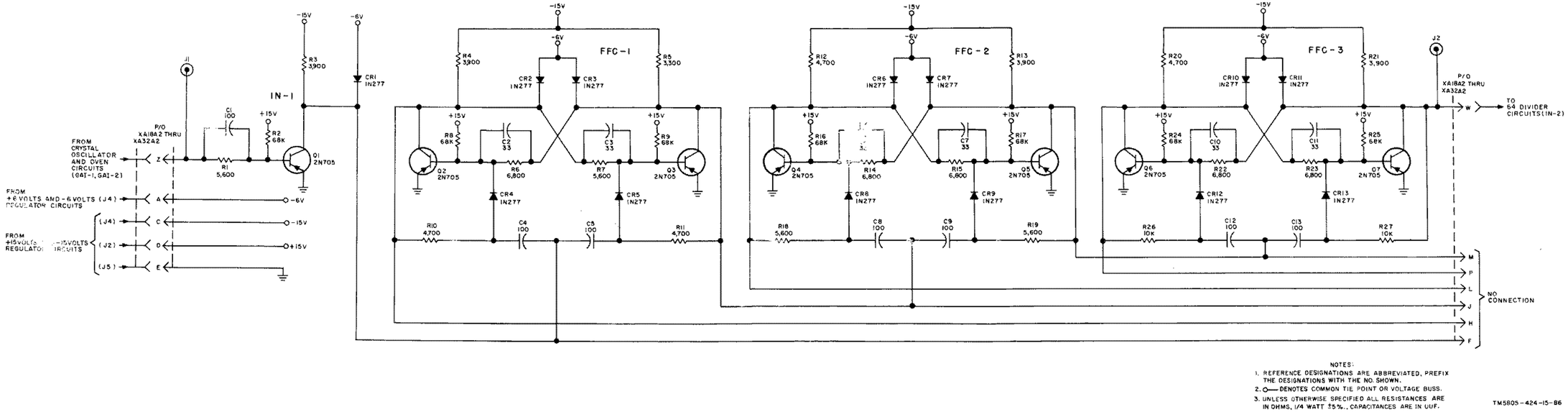


Figure 8-24. Three-stage frequency divider circuit assemblies A18A2 and A19A2 (PC 80034200), schematic diagram.

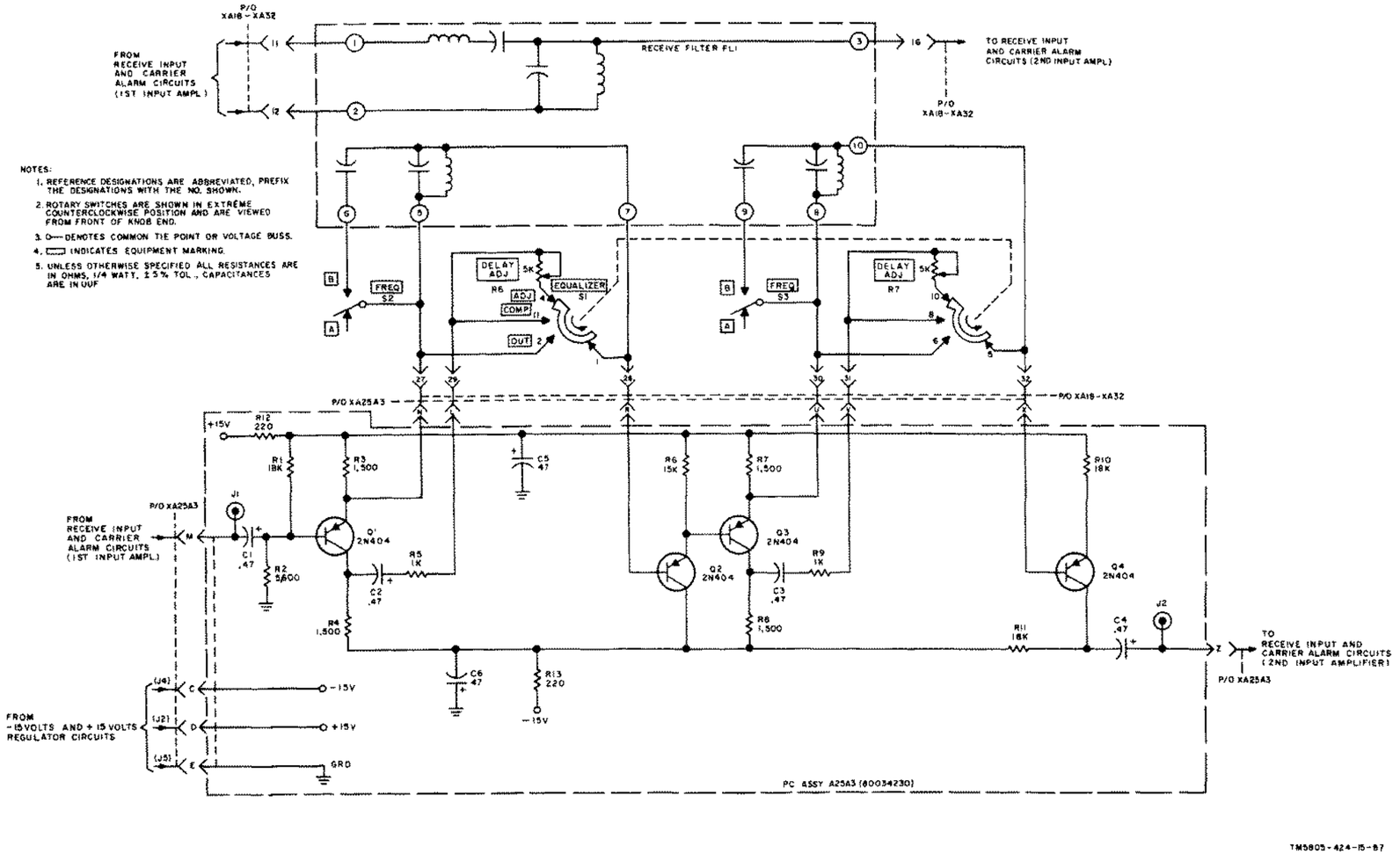


Figure 8-25. Delay equalizer circuits for MX-7379/G (PC 80034230), schematic diagram.

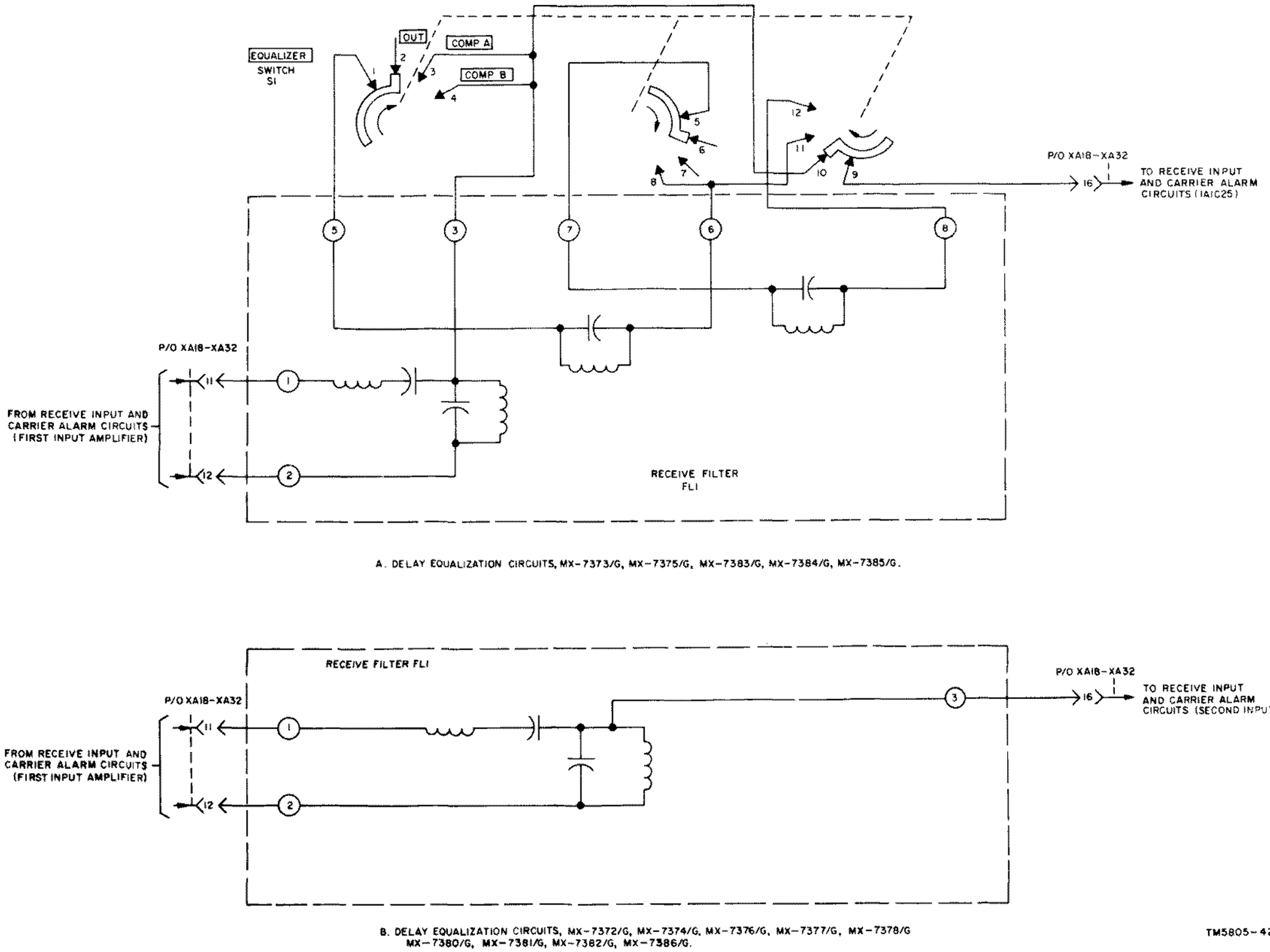


Figure 8-26. Delay equalization circuits (except MX-7379/G) schematic diagrams.

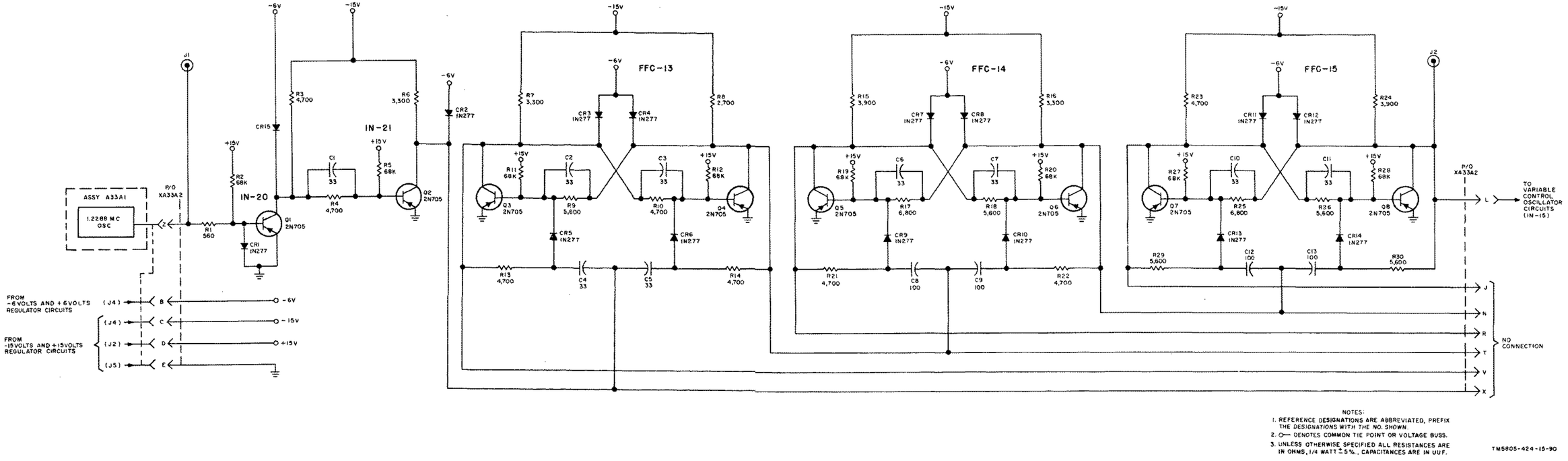


Figure 8-27. Clock divider circuits assembly A33A2 (PC 80034110) schematic diagram.

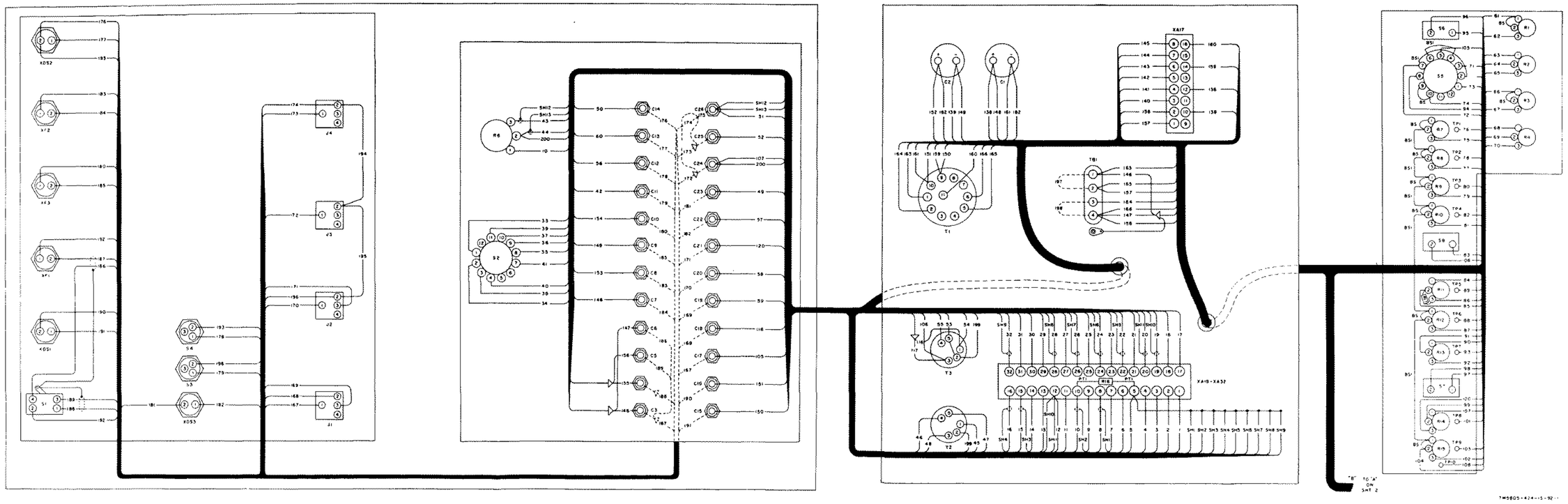


Figure 8-28(1). Modem chassis overall wiring diagram (part 1 of 3).

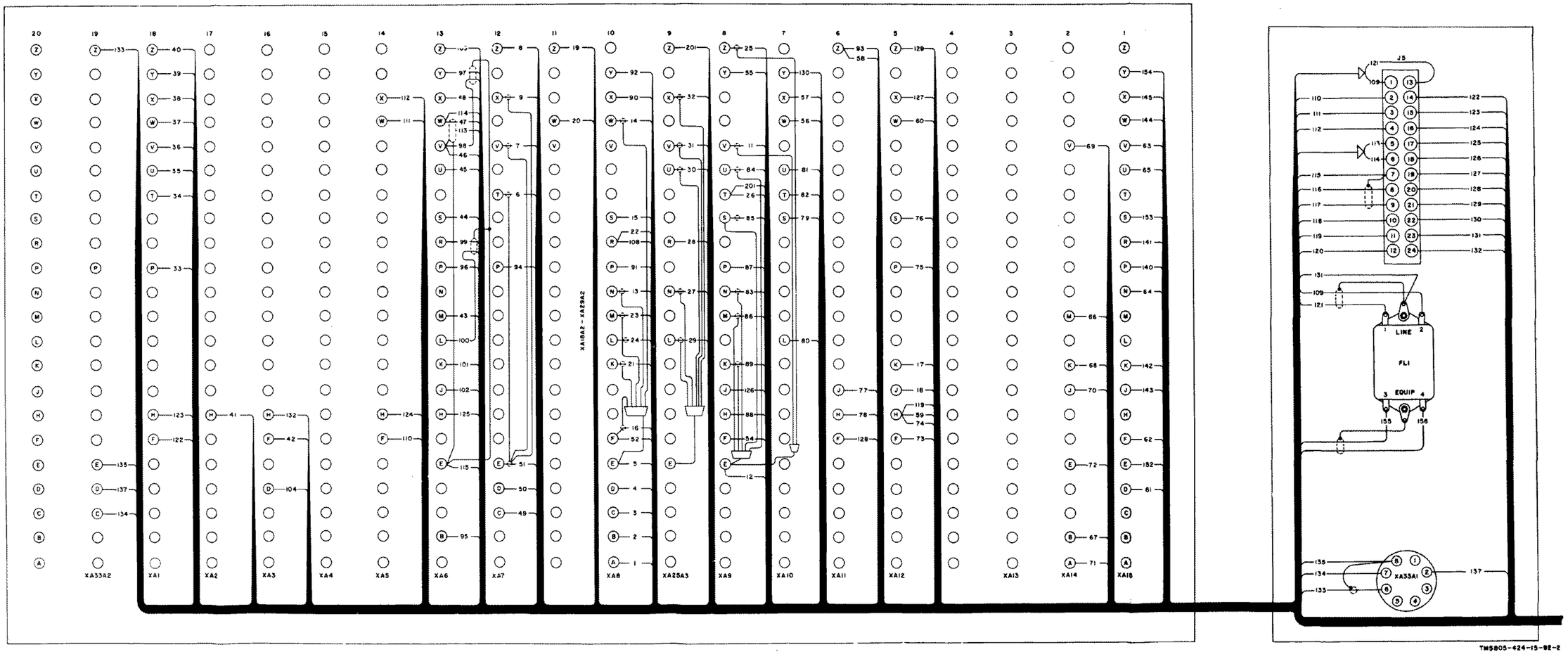


Figure 8-28(2). Modem chassis overall wiring diagram (part 2 of 3).

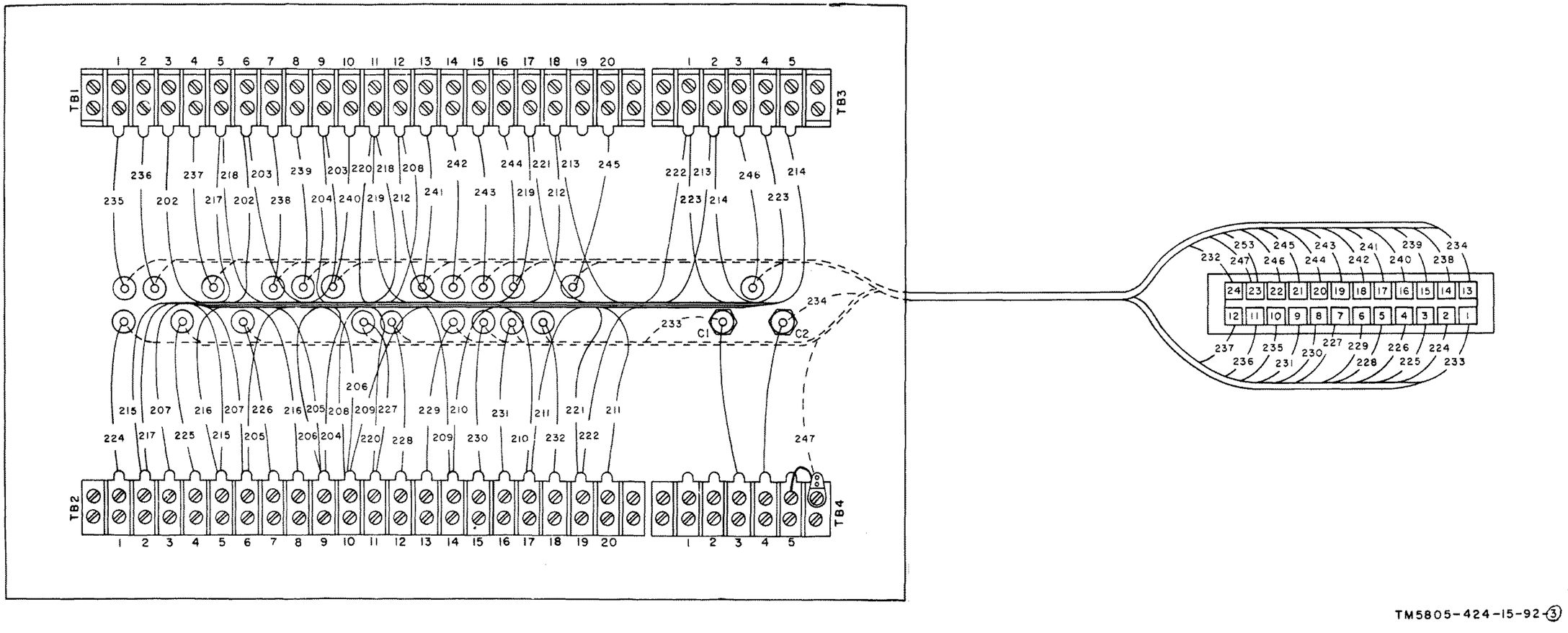


Figure 8-28(3). Modem chassis overall wiring diagram (part 3 of 3).

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The Metric System and Equivalents

Linear Measure

1 centimeter = 10 millimeters = .39 inch
1 decimeter = 10 centimeters = 3.94 inches
1 meter = 10 decimeters = 39.37 inches
1 dekameter = 10 meters = 32.8 feet
1 hectometer = 10 dekameters = 328.08 feet
1 kilometer = 10 hectometers = 3,280.8 feet

Weights

1 centigram = 10 milligrams = .15 grain
1 decigram = 10 centigrams = 1.54 grains
1 gram = 10 decigram = .035 ounce
1 decagram = 10 grams = .35 ounce
1 hectogram = 10 decagrams = 3.52 ounces
1 kilogram = 10 hectograms = 2.2 pounds
1 quintal = 100 kilograms = 220.46 pounds
1 metric ton = 10 quintals = 1.1 short tons

Liquid Measure

1 centiliter = 10 milliters = .34 fl. ounce
1 deciliter = 10 centiliters = 3.38 fl. ounces
1 liter = 10 deciliters = 33.81 fl. ounces
1 dekaliter = 10 liters = 2.64 gallons
1 hectoliter = 10 dekaliters = 26.42 gallons
1 kiloliter = 10 hectoliters = 264.18 gallons

Square Measure

1 sq. centimeter = 100 sq. millimeters = .155 sq. inch
1 sq. decimeter = 100 sq. centimeters = 15.5 sq. inches
1 sq. meter (centare) = 100 sq. decimeters = 10.76 sq. feet
1 sq. dekameter (are) = 100 sq. meters = 1,076.4 sq. feet
1 sq. hectometer (hectare) = 100 sq. dekameters = 2.47 acres
1 sq. kilometer = 100 sq. hectometers = .386 sq. mile

Cubic Measure

1 cu. centimeter = 1000 cu. millimeters = .06 cu. inch
1 cu. decimeter = 1000 cu. centimeters = 61.02 cu. inches
1 cu. meter = 1000 cu. decimeters = 35.31 cu. feet

Approximate Conversion Factors

To change	*To*	*Multiply by*	*To change*	*To*	*Multiply by*
inches	centimeters	2.540	ounce-inches	Newton-meters	.007062
feet	meters	.305	centimeters	inches	.394
yards	meters	.914	meters	feet	3.280
miles	kilometers	1.609	meters	yards	1.094
square inches	square centimeters	6.451	kilometers	miles	.621
square feet	square meters	.093	square centimeters	square inches	.155
square yards	square meters	.836	square meters	square feet	10.764
square miles	square kilometers	2.590	square meters	square yards	1.196
acres	square hectometers	.405	square kilometers	square miles	.386
cubic feet	cubic meters	.028	square hectometers	acres	2.471
cubic yards	cubic meters	.765	cubic meters	cubic feet	35.315
fluid ounces	milliliters	29,573	cubic meters	cubic yards	1.308
pints	liters	.473	milliliters	fluid ounces	.034
quarts	liters	.946	liters	pints	2.113
gallons	liters	3.785	liters	quarts	1.057
ounces	grams	28.349	liters	gallons	.264
pounds	kilograms	.454	grams	ounces	.035
short tons	metric tons	.907	kilograms	pounds	2.205
pound-feet	Newton-meters	1.356	metric tons	short tons	1.102
pound-inches	Newton-meters	.11296			

Temperature (Exact)

°F	Fahrenheit temperature	5/9 (after subtracting 32)	Celsius temperature	°C

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